CP307

3U CompactPCI Processor Board based on the Intel® Core™ Duo Processor and the Intel® Core™2 Duo Processor with the Intel® 945GM Express Chipset

Doc. ID: 34424, Rev. 3.0
December 17, 2008

User Guide

Revision History

Publication Title:	CP307: 3U CompactPCI Processor Board based on the Intel® Core™ Duo Processor and the Intel® Core™2 Duo Processor with the Intel® 945GM Express Chipset	
Doc. ID:	34424	
Rev.	**Brief Description of Changes**	**Date of Issue**
1.0	Initial issue	24-Nov-2006
2.0	General update	10-Aug-2007
3.0	General update, addition of a thermal characteristics graph for the CP307 with the Intel® Core™ Duo processor, 2.0 GHz	17-Dec-2008

Imprint

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Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!

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Caution, Electric Shock!

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Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!

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Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Kontron grants the original purchaser of Kontron's products a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

Kontron warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long-term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter *1*

Introduction

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1. Introduction

1.1 System Overview

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the home page of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system-relevant CompactPCI features that are specific to Kontron CompactPCI systems may be found described in the Kontron CompactPCI System Manual. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine Kontron’s racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of Kontron CompactPCI boards, such as functionality, hot swap capability. In addition, an overview is given for all existing Kontron CompactPCI boards with links to the relating data sheets.
- Generic information on the Kontron CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the Kontron CompactPCI standard backplane family.
- Generic information on the Kontron CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the Kontron CompactPCI standard power supply unit family.

1.2 Board Overview

1.2.1 Board Introduction

The CP307 is a highly integrated, 3U, 4 HP or 8 HP, lead-free CompactPCI system controller board. It has been designed to support the Intel® Core™ Duo and the Intel® Core™2 Duo processors with frequencies ranging from 1.2 GHz up to 2.16 GHz providing 533/667 MHz Front Side Bus (FSB) in 479 µFCBGA packaging.

The Intel® Core™ Duo and the Intel® Core™2 Duo are low-power Dual Core™ processors supporting Intel's Virtualization Technology (VT). The Intel® Core™ Duo consists of two cores and up to 2 MB L2 cache shared by both cores. The Intel® Core™2 Duo consists of two cores, up to 4 MB L2 cache shared by both cores, Intel® Extended Memory 64 Technology (Intel® EM64T), enhanced address range for up to 64 GB memory. The Intel® Core™ Duo and the Intel® Core™2 Duo processors deliver optimized power-efficient computing and outstanding dual-core performance with low power consumption.

The CP307 utilizes the Mobile Intel® 945GM Express Graphics Memory Controller Hub (945GM Express GMCH) and the ICH7-R I/O Controller Hub.

The board includes up to 2 GB of soldered Double Data Rate 2 (DDR2) memory and up to 2 GB of SODIMM socket memory. The memory operates at 533/667 MHz.

The CP307 offers more features and expandability than other CompactPCI boards in its class. The board comes with an onboard SATA port, two Gigabit Ethernet ports (Intel® 82573L), two USB 2.0 ports on the front panel, and a built-in Intel 3D Graphics accelerator for enhanced graphics performance with a VGA analog display interface. A CompactFlash socket for type I and type II CompactFlash cards is provided via the CP307-CF piggy-back module of the CP307. Several onboard connectors provide flexible 8HP expandability.

The board supports one 32-bit/33 MHz CompactPCI interface acting as system master CPU only.

The optional CP307-HDD module has been designed to make various legacy PC I/O ports available as well as DVI and USB interfacing. It includes one COM port, a PS/2 keyboard and mouse port, a 2.5" onboard hard disk SATA interface, a PATA IDE connector (i.e. for a CD/ DVD drive), two USB 2.0 ports, and a DVI-D connector.

Designed for stability and packaged in a rugged format, the board fits into all applications situated in industrial environments, including I/O intensive applications where only one slot is available for the CPU, making it a perfect core technology for long-life applications. Components which have high temperature tolerance have been selected from embedded technology programs, and therefore offer long-term availability.

There are various operating systems available for the CP307. For detailed information, please contact Kontron.

1.2.2 Board-Specific Information

The CP307 is a CompactPCI single-board computer based on Intel's Dual Core™ processor technology and is specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP307's outstanding features are:

- Support for the following processors:
  - Intel® Core™ Duo processor U2500 (ULV), 1.2 GHz, 533 MHz FSB, 2 MB L2 cache
  - Intel® Core™ Duo processor L2400 (LV), 1.66 GHz, 667 MHz FSB, 2 MB L2 cache
  - Intel® Core™ Duo processor T2500 (SV), 2.0 GHz, 667 MHz FSB, 2 MB L2 cache
  - Intel® Core™2 Duo processor L7400 (LV), 1.5 GHz, 667 MHz FSB, 4 MB L2 cache
  - Intel® Core™2 Duo processor T7400 (SV), 2.16 GHz, 667 MHz FSB, 4 MB L2 cache
- 479-pin µFCBGA package
- 64 kB L1 and up to 4 MB L2 cache on-die, running at CPU speed
- 945GM and 82801GR (ICH7R) chipset
- Up to 4 GB DDR2-SDRAM memory running at 533/667 MHz
- Integrated 3D high performance VGA controller
- Analog display support of up to 2048 x 1536 pixels at 75 Hz
- DVI-D option (with 8HP version)
- Two Gigabit Ethernet interfaces (82573L)
- Up to four Serial ATA (SATA) interfaces with SATA RAID 0/1/5/10 support
- One IDE Ultra ATA/100 interface
- Onboard Compact Flash socket for type I and type II CompactFlash cards (True IDE with DMA) on CP307-CF module for 4HP version and CP307-HDD module for 8HP version
- Six USB ports
  - Two Front USB 2.0
  - Two further Front USB 2.0 on the 8HP version
  - Two Rear I/O USB 2.0
- Compatible with CompactPCI Specification PICMG 2.0. Rev. 3.0
- 1 MB onboard FWH for BIOS
- Hardware Monitor (Super I/O SCH3112)
- Watchdog timer
- Real-time clock
- Two COM ports on Rear I/O (with an optional single port on the front I/O on 8HP version)
- I/O extension connectors (SATA, SDVO, USB, PS/2, LPC, IDE, COM, as well as Monitor and Control signals)
- 4HP or 8HP, 3U CompactPCI
- Reset push button switch (with 8HP version)
- Several Rear I/O configurations
- Jumperless board configuration
- Power-up sequencing and in-rush current optimized design
- Passive heat sink solution
- AMI BIOS

1.3 Optional Modules

1.3.1 CP307-HDD Module

The CP307-HDD module for the 8 HP CP307 version provides legacy PC I/O ports. It includes one digital DVI port, two USB 2.0 ports, one COM port, a PS/2 keyboard and mouse port, one IDE connector, and one CompactFlash socket. A SATA hard disk interface is also available for mounting a 2.5” hard disk drive.

Refer to Appendix A for further information on the CP307-HDD module.

1.4 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP307.

Table 1-1: System Relevant Information

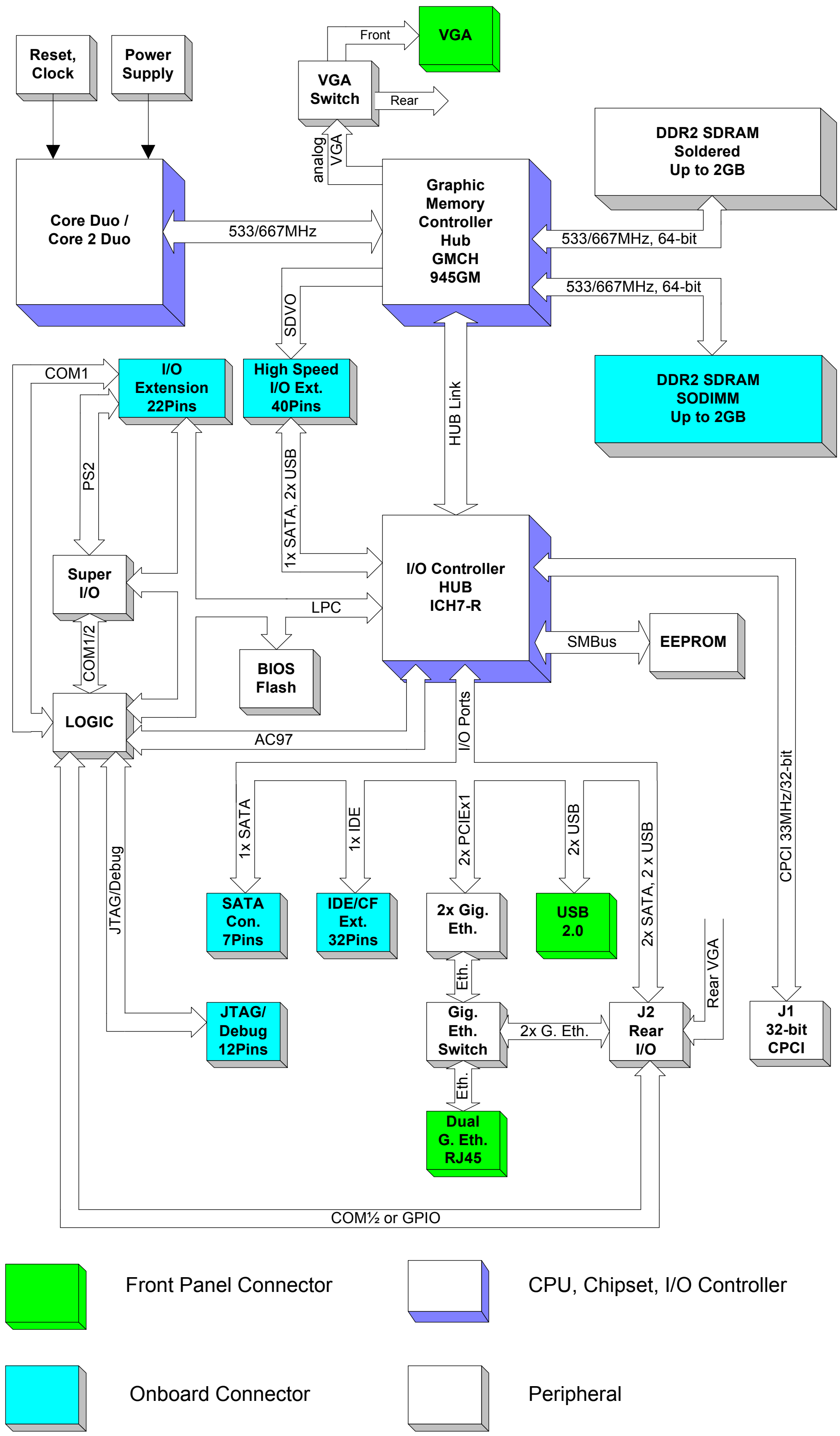
SUBJECT	INFORMATION
System Configuration	The CP307 system controller board can support up to 7 peripheral boards with 32-bit and 33 MHz.
Master/Slave Functionality	The CP307 can operate only as a master board.
Board Location in the System	The CP307 board must be installed in a system slot of a CompactPCI backplane.
Hot Swap Compatibility	The CP307 supports the addition or removal of other boards whilst in a powered-up state. Individual clocks for each slot and ENUM signal handling are in compliance with the PICMG 2.1 Hot Swap specification.
Hardware Requirements	The CP307 can be installed in any CompactPCI 3U rack.
Operating Systems	There are various operating systems available for the CP307. For detailed information, please contact Kontron.

1.5 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

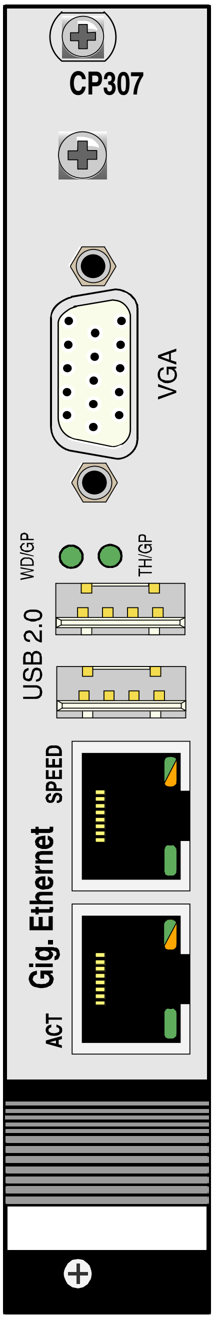
1.5.1 Functional Block Diagram

Figure 1-1: CP307 Functional Block Diagram



1.5.2 Front Panel

Figure 1-2: CP307 4HP Front Panel



LEGEND:

CP307: 4HP version

General Purpose LEDs:

WD/GP (green):	Watchdog or General Purpose; when lit during power-on, it indicates a PCI reset is active.
TH/GP (green):	Overtemperature Status or General Purpose; when lit during power-on, it indicates a power failure.

Note ...

If the WD/GP LED and the TH/GP LED keep flashing during BIOS initialization, a POST code is indicated.

For further information on the blinking intervals of the WD/GP LED and the TH/GP LED refer to section 2.3.1 General Purpose LED Output.

Integral Ethernet LEDs

ACT (green):	Ethernet Link/Activity
SPEED (green/orange):	Ethernet Speed
SPEED ON (orange):	1000 Mbit
SPEED ON (green):	100 Mbit
SPEED OFF:	10 Mbit

Note ...

For detailed information on the 8HP CP307 version, refer to Appendix A, CP307-HDD module.

1.5.3 Board Layout

Figure 1-3: 4 HP CP307 Board Layout (Top View)

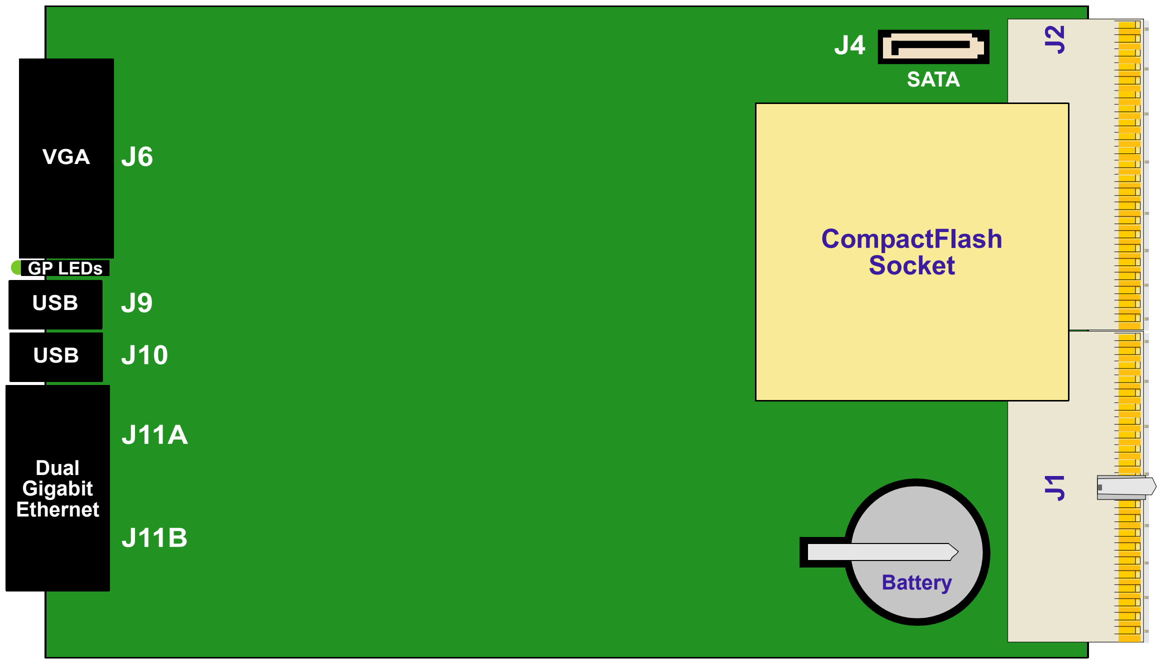
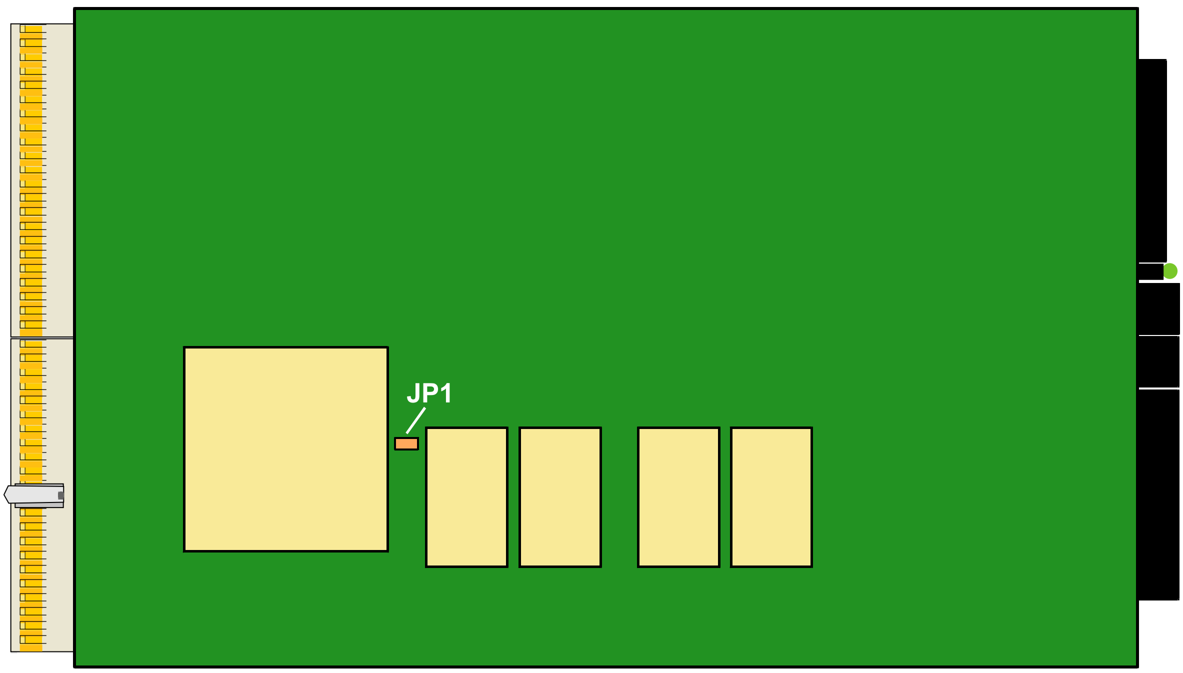


Figure 1-4: 4 HP CP307 Board Layout (Bottom View)



1.6 Technical Specification

Table 1-2: CP307 4HP Version Main Specifications

<table>
<tr><th colspan="2">CP307</th><th>SPECIFICATIONS</th></tr>
<tr><td rowspan="2">Processor and Memory</td><td>CPU</td><td>The CP307 supports the following microprocessors:
• Intel® Core™ Duo
  • Intel® Core™ Duo processor U2500 (ULV), 1.2 GHz, 533 MHz FSB, 2 MB L2 cache
  • Intel® Core™ Duo processor L2400 (LV), 1.66 GHz, 667 MHz FSB, 2 MB L2 cache
  • Intel® Core™ Duo processor T2500 (SV), 2.0 GHz, 667 MHz FSB, 2 MB L2 cache
• Intel® Core™2 Duo
  • Intel® Core™2 Duo processor L7400 (LV), 1.5 GHz, 667 MHz FSB, 4 MB L2 cache
  • Intel® Core™2 Duo processor T7400 (SV), 2.16 GHz, 667 MHz FSB, 4 MB L2 cache
All microprocessors are provided in a 479 μFCBGA packaging.</td></tr>
<tr><td>Memory</td><td>Main Memory:
• Up to 4GB Dual-Channel DDR2 SDRAM memory with one channel soldered and one SODIMM channel.
• 533/667 MHz memory bus
• Error Checking and Correction (ECC) not provided
Cache structure:
• 64 kB L1 on-die full speed processor cache
  • 32 kB for instruction cache
  • 32 kB for data cache
• Up to 4 MB L2 on-die full speed processor cache
FLASH Memory:
• 1 MB FLASH for BIOS
Memory Extension:
• CompactFlash socket for type I and type II CompactFlash cards (true IDE mode)
Serial EEPROM:
• 24LC64 (64 kbit)</td></tr>
</table>

Table 1-2: CP307 4HP Version Main Specifications (Continued)

CP307		SPECIFICATIONS
Chipset	Intel® 945GM Express GMCH	Mobile Intel® 945GM Express Graphics Memory Controller Hub (945GM Express GMCH): • Support for a single Intel® Core™ Duo or Core™2 Duo microprocessor • 64-bit AGTL/AGTL+ based System Bus interface up to 667 MHz • System Memory interface with optimized support for dual-channel DDR2 SDRAM memory at 533/667 MHz without ECC • Integrated 2D and 3D Graphics Engines • Integrated 400 MHz RAMDAC
	Intel® ICH7-R	82801GR I/O Controller Hub (ICH7-R) • PCI Rev. 2.3 compliant with support for 32-bit/33 MHz PCI operations • Power management logic support • Enhanced DMA controller, interrupt controller, and timer functions • Integrated IDE controller Ultra ATA/100/66/33 and PIO mode • USB 2.0 host interface with up to six USB ports available on the CP307 • SATA Host Controller with four ports, 3 Gbit/s transfer rate and RAID 0/1/5/10 support • Two of the six x1 PCI Express ports are used for Gigabit Ethernet • System Management Bus (SMBus) compatible with most I²C™ devices • Low Pin Count (LPC) interface • Firmware Hub (FWH) interface support

Table 1-2: CP307 4HP Version Main Specifications (Continued)

CP307		SPECIFICATIONS

Interfaces	CompactPCI	Compliant with CompactPCI Specification PICMG® 2.0 R 3.0
		• System master operation
		• 32-bit / 33 MHz master interface
		• Signaling voltage fixed either to
		  • 3.3V or
		  • 5V
		The desired signaling voltage must be stated in the order.

	Rear I/O	The following interfaces are routed to the Rear I/O connector J2: • COM1 and COM2 (3.3V TTL signaling) • 2 x USB 2.0 • VGA (analog) • 2x Gigabit Ethernet • 2x SATA (RAID support) • System Management signals • General Purpose signals
	Hot Swap	The CP307 is not hot-swappable but supports the addition and removal of other boards whilst in a powered-up state. Individual clocks for each slot and Enum signal handling are in compliance with the PICMG 2.1 Hot Swap Specification.
	VGA	Built-in Intel 3D Graphics accelerator for enhanced graphics performance. • Supports resolutions of up to 2048 x 1536 at a 75 Hz refresh rate • Hardware motion compensation for software MPEG2 decoding • Dynamic Video Memory Technology (DVMT3.0)
	Gigabit Ethernet	Two 10 Base-T/100 Base-TX/1000 Base-T Gigabit Ethernet interfaces based on the Intel® 82573L Ethernet PCI Express bus controller individually switchable to front or read I/O • Dual RJ-45 connector on the front panel • Automatic mode recognition • Automatic cabling configuration recognition Cabling requirement: Category 5, UTP, four-pair cabling
	USB	Six USB ports supporting UHCI and EHCI: • Two USB 2.0 connectors on the front panel • Two USB 2.0 connectors on the front panel of the 8 HP version • Two USB 2.0 connectors on the Rear I/O interface
	Serial	Two UARTs, 16C550 compatible. • COM1 available either on the front panel of the 8 HP version or on the Rear I/O • COM2 available on Rear I/O only
	Keyboard and Mouse	Keyboard and Mouse are supported • USB keyboard support on 4HP and 8HP • PS/2 only with CP307-HDD module (8HP)

Table 1-2: CP307 4HP Version Main Specifications (Continued)

CP307		SPECIFICATIONS
Interfaces	Mass Storage	SATA: Integrated Serial ATA Host Controllers • One onboard port (SATA connector) • One port available on the CP307-HDD module (8HP) for 2.5” HDD • Two ports available on Rear I/O • Data transfer rate up to 3 Gbit/s • High-performance RAID 0/1/5/10 functionality on all SATA ports IDE Ultra ATA/100/66/33 and PIO • CompactFlash (either on 4 HP or on 8HP) • 40-pin, 2.54 mm, male pinrow connector available on CP307-HDD module (8HP) CompactFlash: • CompactFlash socket for type I and type II CompactFlash cards (DMA capable true IDE mode) • The CompactFlash is always configured as IDE master • Supports type I and II CompactFlash cards 40-pin Standard Connector (only with CP307-HDD module): • If a CompactFlash card is inserted, the drive must be configured as slave (CF is always IDE master).
	I/O extension interfaces	I/O extension interfaces: • SATA • 2x USB2.0 • SDVO • LPC devices • PS/2 • COM1 • Monitor and Control signals
Sockets	Front Panel Connectors	• VGA: 15-pin D-Sub connector • USB: two 4-pin connectors • Ethernet: two RJ-45 connectors
	Onboard Connectors	• One 7-pin, L-form standard SATA connector • I/O extension connectors • One 200-pin SODIMM socket • CompactPCI Connector J1 and J2 • CompactFlash socket for type I, II (on the CP307-CF module)

Table 1-2: CP307 4HP Version Main Specifications (Continued)

CP307		SPECIFICATIONS
HW Monitoring	LEDs	System status: • WD/GP: green: Watchdog or General Purpose; when remains lit during power-on, it indicates PCI reset is active. • TH/GP: green: Overtemperature Status or General Purpose; when remains lit during power-on, it indicates a power failure. Gigabit Ethernet status: • ACT: green: Network/Link Activity • SPEED: green/orange: Network Speed
	Watchdog	Software configurable Watchdog generates IRQ, NMI, or hardware reset.
	Thermal Management	CPU overtemperature protection is provided by: • Internal processor temperature control unit • CPU shut down via hardware monitor • Specially designed heat sink
	System Monitor	Hardware monitor integrated in the SCH3112 for the supervision of: • Several system power voltages • One fan speed input • One fan PWM output • Board temperature
Software	Software BIOS	AMI BIOS with 1 MB Flash memory with the following features: • QuickBoot • QuietBoot • BootBlock • LAN boot capability for diskless systems (standard PXE) • Boot from USB floppy disk drive • BIOS legacy support for USB keyboards • Plug and Play capability • BIOS parameters are saved in the EEPROM • Board serial number is saved within the EEPROM • PC Health Monitoring
	Operating Systems	There are various operating systems available for the CP307. For detailed information, please contact Kontron.

Table 1-2: CP307 4HP Version Main Specifications (Continued)

CP307		SPECIFICATIONS
General	Mechanical	3U, 4HP, CompactPCI compliant form factor
	Power Consumption	Dual Core LV 1.66GHz and 2GB memory: typ. 23W For further information, refer to Chapter 5.
	Temperature Range	Operational: 0°C to +60°C Standard (depending on processor version and airflow in the system) -40°C to +85°C E2 (only with Core™ Duo 1.2 GHz; without hard disk and in the appropriate system environment) Storage: -55°C to +85°C Without hard disk and without battery -40°C to +65°C With hard disk and without battery ***Note ...*** When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CP307 (See "Battery" below). ***Note ...*** When additional components are installed, refer to their operational specifications as this will influence the board's operational and storage temperature.
	Heat Sink	Depending on the processor used, there are two types of heat sinks available with the CP307: • Aluminum heat sink for the CP307 with Core™ Duo 1.2 GHz, Core™ Duo 1.66 GHz and Core™2 Duo 1.5 GHz • Copper heat sink for the CP307 with Core™ Duo 2.0 GHz and Core™2 Duo 2.16 GHz
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 160 mm
	Board Weight	320 grams (4HP variants with heat sink, with front panel but without SODIMM module and without mezzanine boards)
	Battery	3.0V lithium battery for RTC with battery socket. Recommended type: CR2025 Temperature ranges: Operational (load): -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage (no load): -55°C to +70°C typical (no discharge)

Note ...

For a description of the additional 8HP version interfaces, refer to the Technical Specifications table in Appendix A, CP307-HDD module.

1.7 Kontron Software Support

Kontron is one of the few CompactPCI and VME vendors providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

1.8 Standards

This Kontron product complies with the requirements of the following standards.

Table 1-3: Standards

TYPE	ASPECT	STANDARD	REMARKS
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950-1	--
Mechanical	Mechanical Dimensions	IEEE1101.10	--
Environmental	Vibration (Sinusoidal)	IEC60068-2-6	5g/10-300Hz/10 acceleration / frequency range / 10 cycles per axis
	Random Vibration (Broadband)	IEC60068-2-64 (3U boards)	20-500Hz,0.05g²/500-2000Hz, 0.005g²/3.5g rms/30min./axis frequency range1 / frequency range2 / acceleration / cycle / duration
	Permanent Shock	IEC60068-2-29	15g/11ms/500/1s peak acceleration / shock duration half sine / number of shocks / recovery time
	Single Shock	IEC60068-2-27	30g/9ms/18/5s peak acceleration / shock duration / number of shocks / recovery time in seconds
	Climatic Humidity	IEC60068-2-78	93% RH at 40°C, non-condensing
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS	Directive 2002/95/EC	Restriction of the use of certain hazardous substances in electrical and electronic equipment

Note ...

The values in the above table are valid for boards which are ordered with the ruggedized service. For further information, please contact your local Kontron office.

1.9 Related Publications

The following publications contain information relating to this product.

Table 1-4: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification PICMG 2.0, Rev. 3.0 CompactPCI System Management Specification PICMG 2.9 Rev. 1.0 CompactPCI Hot Swap Specification PICMG 2.1 Rev. 2.0
	Hot Swap Specification PICMG 2.1
	Kontron's CompactPCI System Manual, ID 19954
CompactFlash Cards	CF+ and CompactFlash Specification Revision 2.0
Serial ATA	Serial ATA 1.0a Specification

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Chapter 2

Functional Description

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2. Functional Description

2.1 CPU, Memory and Chipset

2.1.1 CPU

The CP307 supports the latest Intel® Core™ Duo and Intel® Core™2 Duo processor family up to speeds of 2.16 GHz with up to 667 MHz FSB.

The Intel® Core™ Duo consists of two cores and up to 2 MB L2 cache shared by both cores. The Intel® Core™2 Duo consists of two cores, up to 4 MB L2 cache shared by both cores, Intel® Extended Memory 64 Technology (Intel® EM64T), and enhanced address range for up to 64 GB memory. The Intel® Core™ Duo and the Intel® Core™2 Duo processors deliver optimized power-efficient computing and outstanding dual-core performance with low power consumption.

The Intel® Core™ Duo and the Intel® Core™2 Duo support the latest Intel's Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions, such as performing system upgrades and maintenance without interrupting the system or the application, keeping software loads and virus attacks separate, combining multiple servers in one system, etc. With processor and I/O enhancements to Intel's various platforms, Intel Virtualization Technology improves the performance and robustness of today's software-only virtual machine solutions.

Furthermore, the Intel® Core™ Duo and the Intel® Core™2 Duo also support the Intel® SpeedStep® technology which enables real-time dynamic switching of the voltage and frequency between several modes. This is achieved by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system. The frequency for the processor may also be selected in the BIOS or via the operating system.

The following list sets out some of the key features of the Intel® Core™ Duo and the Intel® Core™2 Duo processors:

- Two mobile execution cores in one single processor
- Support of Intel's Virtualization Technology (Vanderpool)
- Support of Intel Architecture with Dynamic Execution
- Outstanding dual-core performance with low power consumption
- On-die, primary 32 kB instruction cache and 32 kB write-back data cache
- On-die, L1 and L2 cache with Advanced Transfer Cache Architecture
  - Intel® Core™ Duo processor U2500 (ULV), 1.2 GHz, 533 MHz FSB, 2 MB L2 cache
  - Intel® Core™ Duo processor L2400 (LV), 1.66 GHz, 667 MHz FSB, 2 MB L2 cache
  - Intel® Core™ Duo processor T2500 (SV), 2.0 GHz, 667 MHz FSB, 2 MB L2 cache
  - Intel® Core™2 Duo processor L7400 (LV), 1.5 GHz, 667 MHz FSB, 4 MB L2 cache
  - Intel® Core™2 Duo processor T7400 (SV), 2.16 GHz, 667 MHz FSB, 4 MB L2 cache
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 3 (SSE3)
- Up to 667 MHz, Source-Synchronous Front Side Bus (FSB)
- Advanced Power Management features including Enhanced Intel® SpeedStep® technology
- Intel® Extended Memory 64 Technology for 64-bit computing (only with the Intel® Core™2 Duo)

The following tables provide information about the Intel® Core™ Duo and the Intel® Core™2 Duo processors supported on the CP307.

Table 2-1: Processors Supported on the CP307

SPEED	Core™ Duo 1.2 GHz (ULV[1]) 2 MB L2 Cache	Core™ Duo 1.66 GHz (LV[2]) 2 MB L2 Cache	Core™ Duo 2.0 GHz (SV[3]) 2 MB L2 Cache	Core™2 Duo 1.5 GHz (LV[2]) 4 MB L2 Cache	Core™2 Duo 2.16 GHz (SV[3]) 4 MB L2 Cache
PACKAGE	µFCBGA	µFCBGA	µFCBGA	µFCBGA	µFCBGA
L2 CACHE	2 MB	2 MB	2 MB	4 MB	4 MB
FSB	533 MHz	667 MHz	667 MHz	667 MHz	667 MHz

[1]ULV: Ultra Low Voltage
[2]LV: Low Voltage
[3]SV: Standard Voltage

Table 2-2: Maximum Power Dissipation of the Processors (CPU only)

FREQUENCY MODE	Core™ Duo 1.2 GHz (ULV) 2 MB L2 Cache	Core™ Duo 1.66 GHz (LV) 2 MB L2 Cache	Core™ Duo 2.0 GHz (SV) 2 MB L2 Cache	Core™2 Duo 1.5 GHz (LV) 4 MB L2 Cache	Core™2 Duo 2.16 GHz (SV) 4 MB L2 Cache
Maximum Power HFM[4]	9.0 W	15 W	31 W	17 W	34 W
Maximum Power LFM[5]	7.5 W	13 W	13 W	15 W	20 W

[4]HFM: High Frequency Mode (maximum frequency of the CPU)
[5]LFM: Low Frequency Mode (frequency is 1.0 GHz for 667 MHz FSB and 800 MHz for 533 MHz FSB)

Table 2-3: CPU Frequency in the Various SpeedStep® Modes

FREQUENCY	Core™ Duo 1.2 GHz (ULV) 2MB L2 Cache	Core™ Duo 1.66 GHz (LV) 2 MB L2 Cache	Core™ Duo 2.0 GHz (SV) 2 MB L2 Cache	Core™2 Duo 1.5 GHz (LV) 4 MB L2 Cache	Core™2 Duo 2.16 GHz (SV) 4 MB L2 Cache
2.16 GHz	--	--	--	--	x
2.0 GHz	--	--	x	--	--
1.66 GHz	--	x	x	--	x
1.5 GHz	--	--	--	x	--
1.33 GHz	--	x	x	--	x
1.2 GHz	x	--	--	--	--
1.0 GHz	--	x	x	x	x
800 MHz	x	--	--	--	--

2.1.2 Memory

The CP307 supports a dual-channel DDR2 memory without Error Checking and Correcting (ECC) running at 667 MHz (PC2-5300-CL5). Channel A is soldered. Channel B provides one 200-pin SODIMM socket for a DDR2 SODIMM module. The maximum memory size per channel is 2 GB. The available memory module configuration can be either 512 MB, 1 GB, 2 GB, or 4 GB. However, due to internal memory allocations, the amount of memory available to applications is less than the total physical memory in the system. For example, the chipset's Dynamic Video Memory Technology (DVMT 3.0) dynamically allocates the proper amount of system memory required by the operating system and the application.

Table 2-4: Supported Memory Configurations

CHANNEL A (SOLDERED)	CHANNEL B (SODIMM)	TOTAL PHYSICAL MEMORY	TOTAL MEMORY AVAILABLE TO APPLICATIONS
512 MB	--	512 MB	512 MB minus the allocated memory for DVMT
512 MB	512 MB	1 GB	1 GB minus the allocated memory for DVMT
1 GB	--	1 GB	1 GB minus the allocated memory for DVMT
1 GB	1 GB	2 GB	2 GB minus the allocated memory for DVMT
2 GB	--	2 GB	2 GB minus the allocated memory for DVMT
2 GB	2 GB	4 GB	4 GB minus the allocated memory for DVMT, PCI/PCIe devices and the video controller memory address space of 256 MB If the onboard video controller is disabled, the maximum available memory is 3.5 GB. If the onboard video controller is enabled, the maximum available memory is 3.25 GB.

Note ...

Only qualified DDR2 SODIMM modules from Kontron are authorized for use with the CP307.

Warning!

Memory configuration changes are only permitted to be performed at the factory.

Failure to comply with the above may result in damage to your board or improper operation.

2.1.3 Intel® 945GM Express Chipset Overview

The Intel® 945GM Express Chipset consists of the following devices:

- Mobile Intel® 945GM Express Graphics Memory Controller Hub (945GM Express GMCH)
- I/O Controller Hub 7 (ICH7-R)

The 945GM Express GMCH provides the processor interface for the Intel® Core™ Duo and the Intel® Core™2 Duo microprocessors and two DDR2 channels, and includes a high performance graphics accelerator. The ICH7-R is a centralized controller for the boards' I/O peripherals, such as the PCI, PCI Express, USB 2.0, SATA II, IDE and LPC ports.

2.1.4 Mobile Intel® 945GM Express Graphics Memory Controller Hub

The Mobile Intel® 945GM Express Graphics Memory Controller Hub (945GM Express GMCH) is a highly integrated hub that provides the CPU interface (optimized for the Intel® Core™ Duo and the Intel® Core™2 Duo microprocessors), two DDR2 SDRAM system memory interfaces at 533MHz or 667 MHz, a hub link interface to the ICH7-R and high performance internal graphics.

Graphics and Memory Controller Hub Feature Set

Host Interface

The 945GM Express GMCH is optimized for the Intel® Core™ Duo and the Intel® Core™2 Duo microprocessors. The chipset supports a Front Side Bus (FSB) frequencies of 533 MHz or 667 MHz using 1.05 V AGTL signalling. The AGTL bus supports 32-bit host addressing for decoding up to 4 GB memory address space.

System Memory Interface

The 945GM Express GMCH integrates a dual-channel DDR2 SDRAM controller with two 64-bit wide interfaces without ECC bits. The chipset supports DDR533 and DDR667 DDR2 SDRAM for system memory.

945GM Express GMCH

The 945GM Express GMCH includes a highly integrated graphics accelerator delivering high performance 3D and 2D graphic capabilities. The internal graphics controller provides an interface for a standard VGA analog display.

2.1.5 I/O Controller Hub ICH7-R

The ICH7-R is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI Bus and integrates many of the functions needed in today's PC platforms, for example, PCI Express, Ultra DMA 100/66/33 IDE controller, SATA controller with RAID support, USB host controller supporting USB 2.0, LPC interface, and a FWH Flash BIOS interface controller. The ICH7-R communicates with the host controller over a dedicated hub interface.

I/O Controller Hub Feature set comprises:

- PCI 2.3 interface with eight PCI IRQ inputs
- Bus master IDE controller UltraDMA 100/66/33 or PIO mode
- Five USB controllers with up to eight USB 1.1 or USB 2.0 ports (max. of 6 ports available)
- Hub interface for the 945GM Express Chipset
- FWH interface
- LPC interface
- RTC controller

2.2 Peripherals

The following standard peripherals are available on the CP307 board:

2.2.1 Timer

The CP307 is equipped with the following timers:

- Real-Time Clock
  The ICH7-R contains a MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM.
  The real-time clock performs timekeeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. Features include an alarm function, programmable periodic interrupt and a 100-year calendar. All battery-backed CMOS RAM data remains stored in an additional EEPROM. This prevents data loss in case the CP307 is operated without battery.
- Counter/Timer
  Three 8254-style counter/timers are included on the CP307 as defined for the PC/AT.
- In addition to the three 8254-style counters, the ICH7-R includes three individual multimedia event timers that may be used by the operating system. They are implemented as a single counter each with its own comparator and value register.
- Hardware delay timer for short reliable delay times

2.2.2 Watchdog Timer

The CP307 provides a Watchdog Timer that is programmable for a timeout period ranging from 125 ms to 256 s in 12 steps. Failure to trigger the Watchdog Timer in time results in a system reset, an interrupt, or NMI. In the dual-stage mode, a combination of both NMI, and reset if the Watchdog is not serviced. A hardware status flag will be provided to determine if the Watchdog Timer generated the reset.

2.2.3 Battery

The CP307 is provided with a 3.0 V "coin cell" lithium battery for the RTC.

Note ...

If a CP307-HDD module is used on the CP307, either the CP307 or the CP307-HDD module may be equipped with a battery.

Using one battery on the CP307 and one on the CP307-HDD module simultaneously may result in premature discharge of the batteries.

To replace the battery, proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery type is CR2025.

Note ...

The user must be aware that the battery's operational temperature range is less than the CP307's storage temperature range (see Table 1-2).

For exact range information, refer to the battery manufacturer's specifications.

Note ...

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

The typical life expectancy of a 170 mAh battery (CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.

To ensure that the lifetime of the battery has not been exceeded, it is recommended to exchange the battery after 4 - 5 years.

2.2.4 Reset

The CP307 is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.45 V for the 5 V line and below 2.8 V for the 3.3 V line. Other reset sources include the watchdog timer and the local push-button switch (only on 8HP). The CP307 responds to any of these sources by initializing local peripherals.

A reset will be generated by the following conditions:

- +5 V supply falls below 4.45 V (typ.)
- +3.3 V supply falls below 2.8 V (typ.)
- Pushbutton "RESET" pressed (only on 8HP)
- Watchdog overflow
- CompactPCI backplane PRST# input (CompactPCI connector J2, pin C17)

Note ...

The Intel 82801GR chipset provides an enhanced reset control logic. The reset pulse width is typical 5 ms (min. 1 ms) regardless of how long the RESET pushbutton is being pressed or the PRST signal remains active.

2.2.5 SMBus Devices

The CP307 provides a System Management Bus (SMBus) for access to several system monitoring and configuration functions. The SMBus consists of a two-wire I^2C bus interface. The following table describes the function and address of every onboard SMBus device.

Table 2-5: SMBus Device Addresses

DEVICE	SMBUS ADDRESS
EEPROM 24LC64	1010111xb
Clock	1101001xb
SPD (soldered DDR2)	1010000xb
SPD (SODIMM DDR2)	1010010xb

2.2.6 Thermal Management/System Monitoring

The Super I/O SCH3112 can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds and temperatures, all of which are very important for the proper operation and stability of a high-end computer system. The SCH3112 provides an LPC bus interface.

The voltages +12 V, +5 V, +3.3 V, +2.5 V, and Vcore are supervised. One fan tachometer output can be measured using the SCH3112's FAN1 input. One pulse width modulation (PWM1) output can be used for FAN speed control.

The temperature sensors on the SCH3112 monitor the CPU temperature and the ambient temperature around the SCH3112 to ensure that the system is operating at a safe temperature level.

2.2.7 Serial EEPROM

This EEPROM is connected to the SMBus/I²C bus provided by the ICH7-R.

Table 2-6: EEPROM Address Map

ADDRESS	FUNCTION
0x000 - 0x0FF	CMOS backup
0x100 - 0x1FF	Production data
0x200 - 0x3FF	OS Bootparameter
0x400 - 0x1FFF	User

2.2.8 FLASH Memory

There are two flash device interfaces available as described below, one for the BIOS and one for the CompactFlash socket.

2.2.8.1 BIOS FLASH (Firmware Hub)

For simple BIOS updating a standard onboard 1 MB Firmware Hub device is used.

The FWH stores both the system BIOS and graphics BIOS. It can be updated as new versions of the BIOS become available.

2.2.8.2 CompactFlash Socket

A CompactFlash mezzanine adapter CP307-CF is installed on the CP307 4HP versions to provide CompactFlash interfacing.

CompactFlash is a very small removable mass storage device. It provides true IDE functionality compatible with the 16-bit ATA/ATAPI-4 interface.

The CompactFlash socket is connected to the IDE port of the ICH7-R and is set to master configuration.

The CP307 supports DMA and both CF type I and CF type II.

Figure 2-1: CompactFlash Socket

The following table provides the pinout for the CompactFlash connector on the CP307-CF module.

Table 2-7: CompactFlash Connector Pinout

I/O	FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION	I/O
--	Ground Signal	GND	1	2	D03	Data 3	I/O
I/O	Data 4	D04	3	4	D05	Data 5	I/O
I/O	Data 6	D06	5	6	D07	Data 7	I/O
O	Chip Select 0	IDE_CS0	7	8	GND (A10)	--	--
--	--	GND (ATASEL)	9	10	GND (A09)	--	--
--	--	GND (A08)	11	12	GND (A07)	--	--
--	Power 3.3 V	VCC	13	14	GND (A06)	--	--
--	--	GND (A05)	15	16	GND (A04)	--	--
--	--	GND (A03)	17	18	A02	Address 2	O
O	Address 1	A01	19	20	A00	Address 0	O
I/O	Data 0	D00	21	22	D01	Data 1	I/O
I/O	Data 2	D02	23	24	NC (IOCS16)	--	--
--	--	NC (CD2)	25	26	NC (CD1)	--	--
I/O	Data 11	D11	27	28	D12	Data 12	I/O
I/O	Data 13	D13	29	30	D14	Data 14	I/O
I/O	Data 15	D15	31	32	IDE_CS1	Chip Select 1	O
--	--	NC (VS1)	33	34	IORD	I/O Read	O
O	I/O Write	IOWR	35	36	VCC (WE)	Power 3.3 V	--
I	Interrupt Request	INTRQ	37	38	VCC	Power 3.3 V	--
O	Master/Slave	CSEL (GND/pull-up)	39	40	NC (VS2)	--	--
O	Reset	Reset	41	42	IORDY	I/O Ready	I
I	DMA Request	DMARQ	43	44	DMACK	DMA Acknowledge	O
--	--	NC (DASP)	45	46	PDIAG#/ CBLID#*	Detect ATA100	I
I/O	Data 08	D08	47	48	D09	Data 09	I/O
I/O	Data 10	D10	49	50	GND	Ground Signal	--

* Signal terminated with 10 kΩ pull-down resistor

2.3 Board Interfaces

2.3.1 General Purpose LED Output

The CP307 provides two software programmable GP LEDs. After reset the default configuration for the two front LEDs is Overtemperature and Watchdog status. Additionally, if the WD LED remains on during power-on, it indicates a PCI reset is active, and if the TH LED remains on during power-on, it indicates a power failure. In this case, please check the power supply. If the power supply appears to be functional and the LED remains on, please contact Kontron.

If the WD/GP LED and the TH/GP LED keep flashing during BIOS initialization, a POST code is indicated. For information on the POST Codes, refer to the CP307 BIOS Guide, Chapter 10, POST Codes.

The following table defines the blinking intervals of the WD/GP LED and the TH/GP LED.

Table 2-8: POST Code Indication

LED	NUMBER OF BLINKS
WD/GP LED	high-order nibble (bits 4-7) of POST code
TH/GP LED	low-order nibble (bits 0-3) of POST code

For example, if the WD/GP LED blinks 13 times and the TH/GP LED blinks 5 times, the POST code is 0xD5.

Furthermore, the WD/GP LED and the TH/GP LED can be configured via two onboard registers. For further information refer to Chapter 4 Configuration.

The LED control logic remains in the same state until the next system reset.

Note ...

If the TH/GP LED (overtemperature LED) flashes at regular intervals, it indicates that the processor or the 945GM Express GMCH junction temperature has reached a level beyond which permanent silicon damage may occur. Upon assertion of Thermtrip, the devices will shut off their internal clocks (thus halting program execution) in an attempt to reduce the junction temperature.

Once activated, Thermtrip remains latched until a cold restart of the CP307 is undertaken (all power off and then on again).

2.3.2 USB Interfaces

The CP307 supports six USB 2.0 ports (two front I/O, two front I/O on the 8HP version, and two on the Rear I/O module). On the USB 2.0 Rear I/O ports, it is strongly recommended to use a cable below 3 meters in length for USB 2.0 devices. The USB 2.0 ports are high-speed, full-speed, and low-speed capable. Hi-speed USB 2.0 allows data transfers of up to 480 Mb/s - 40 times faster than a full-speed USB (USB 1.1).

One USB peripheral may be connected to each port.

To connect more USB devices than there are available ports, an external hub is required.

Figure 2-2: USB Connectors J9 and J10

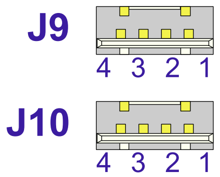


Table 2-9: USB Connectors J9 and J10 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND	--

Note ...

The CP307 host interfaces can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

2.3.3 Graphics Controller

The 945GM Express GMCH includes a highly integrated graphics accelerator delivering high performance 3D, 2D graphics capabilities. The internal graphics controller has two independent display pipes allowing for support of two independent display screens.

Integrated 2D/3D Graphics:

- Intel® Gen3.5 integrated graphics engine
- Smart 2D display technology (S2DDT)
- Dynamic video memory technology
- Integrated 400 MHz RAMDAC
- Resolution up to 2048 x 1536 pixels @ 75 Hz (QXGA)
- Integrated H/W Motion Compensation for MPEG2 decode

2.3.3.1 Graphics Memory Usage

The 945GM Express GMCH supports the Dynamic Video Memory Technology (DVMT 3.0). This technology ensures the most efficient use of all available memory for maximum 3D graphics performance. DVMT dynamically responds to application requirements allocating display and texturing memory resources as required.

The graphics controller is fed with data from the 945GM memory controller. The graphics performance is directly related to the amount of memory bandwith available.

2.3.3.2 Graphics Resolution

The 945GM Express GMCH has an integrated 400 MHz RAMDAC that can directly drive a progressive scan analog monitor up to a resolution of 2048 x 1536 pixels @ 75 Hz.

2.3.3.3 VGA Analog Interface and Connector J6

The 15-pin female connector J6 is used to connect a VGA analog monitor to the CP307 board.

Figure 2-3: D-Sub VGA Con. J6

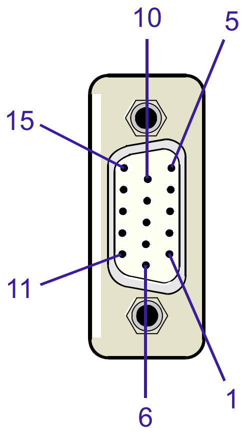


Table 2-10: D-Sub VGA Connector J6 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	Red	Red video signal output	O
2	Green	Green video signal output	O
3	Blue	Blue video signal output	O
10*	VGA_DETECT	Monitor detection signal	I
13	Hsync	Horizontal sync.	TTL Out
14	Vsync	Vertical sync.	TTL Out
12	Sdata	I^2C data	I/O
15	Sclk	I^2C clock	I/O
9	VCC	Power +5V, 1.5 A fuse protection	O
5,6,7,8	GND	Ground signal	--
4,11	NC	--	--

* Pin 10 is normally defined as Ground but is used on the CP307 as detection signal of a connected monitor if the BIOS setting for the CP307 is "AUTO" (the BIOS default setting is "FRONT").

Note ...

If the automatic VGA detection mechanism on the CP307 is used, the user must ensure that the VGA cable and the connected monitor have a GND signal on pin 10. Otherwise the interface is not operable.

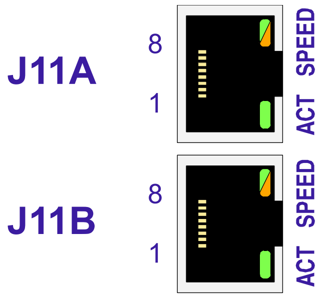
2.3.4 Gigabit Ethernet

The CP307 board includes two 10Base-T/100Base-TX/1000Base-T Ethernet ports based on two Intel® 82573L Gigabit Ethernet controllers, which are connected to the x1 PCI Express interfaces of the ICH7-R.

The Intel® 82573L Gigabit Ethernet Controller's architecture is optimized to deliver high performance with the lowest power consumption. The controller's architecture includes independent transmit and receive queues and a PCI Express interface that maximizes the use of bursts for efficient bus usage.

The Boot from LAN feature is supported.

Figure 2-4: Dual Gigabit Ethernet Connector J11A/B



Note ...

The Ethernet transmission can operate effectively using a CAT5 cable with a maximum length of 100 m.

The Ethernet connectors are realized as RJ-45 connectors. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

RJ-45 Connector J11A/B Pinouts

The J11A/B connector supplies the 10Base-T, 100Base-TX and 1000Base-T interfaces to the Ethernet controller.

Table 2-11: Pinouts of J11A/B Based on the Implementation

MDI / STANDARD ETHERNET CABLE						PIN	MDIX / CROSSED ETHERNET CABLE					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	RX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

Ethernet LED Status

ACT (green): This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ-45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

SPEED (green/orange): This LED lights up to indicate a successful 100Base-TX or 1000BASE-T connection. When lit green, it indicates a 100Base-TX connection and when lit orange it indicates a 1000Base-T connection. When not lit and the ACT-LED is active, the connection is operating at 10Base-T.

2.3.5 Serial ATA Connector J4 (SATA0)

The CP307 is equipped with a SATA connector, J4, which is used to connect standard HDDs and other SATA devices to the CP307.

Figure 2-5: SATA Connector J4

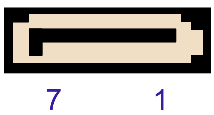


Table 2-12: SATA Connector J4 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	GND	Ground signal	--
2	SATA_TX0+	Differential Transmit +	O
3	SATA_TX0-	Differential Transmit -	O
4	GND	Ground signal	--
5	SATA_RX0-	Differential Receive -	I
6	SATA_RX0+	Differential Receive +	I
7	GND	Ground signal	--

Note ...

The onboard SATA interface supports SATA I (1.5 Gbit/sec) and SATA II (3.0 Gbit/sec).

Note ...

To ensure secure connectivity, the SATA connector supports the use of SATA II cables (SATA cables with locking latch).

2.3.6 CompactPCI Bus Interface

The complete CompactPCI connector configuration comprises two connectors named J1 and J2.

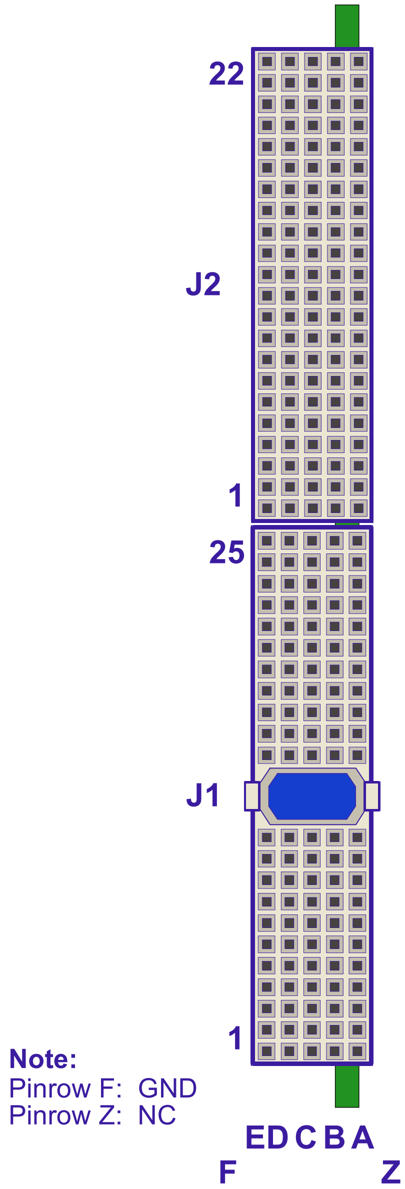
Their function is as follows:

- J1: 32-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J2: arbitration, clock and optionally either Rear I/O interface functionality or 64-bit termination

The board is capable of driving up to seven CompactPCI slots, with individual arbitration and clock signals. The CP307 is not hot-swappable but supports the addition or removal of other boards whilst in a powered-up state.

The CP307 is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

Figure 2-6: CPCI Connectors J1/J2



2.3.6.1 CompactPCI Connector Keying

CompactPCI connectors support guide lugs to ensure a correct polarized mating. A proper mating is further assured by the use of color coded keys for 3.3 V and 5 V operation.

Color coded keys prevent inadvertent installation of a 5 V board into a 3.3 V slot and vice versa. The CP307 board may be ordered as either a 3.3 V or a 5 V version. Backplane connectors are always keyed according to the signaling (VIO) level. Coding key colors are defined as follows:

Table 2-13: Coding Key Colors

SIGNALING VOLTAGE	KEY COLOR
3.3 V	Cadmium Yellow
5 V	Brilliant Blue

2.3.6.2 CompactPCI Connectors J1 and J2 Pinouts

The CP307 is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 2-14: CompactPCI Bus Connector J1 Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
25	NC	5V	REQ64#	ENUM#	3.3V	5V	GND
24	NC	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	NC	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	NC	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	NC	3.3V	AD[9]	AD[8]	M66EN#	C/BE[0]#	GND
20	NC	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	NC	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	NC	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	NC	3.3V	NC	NC	GND	PERR#	GND
16	NC	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	NC	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
12-14	Key Area						
11	NC	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	NC	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	NC	C/BE[3]#	NC	AD[23]	GND	AD[22]	GND
8	NC	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	NC	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	NC	REQ0#	GND	3.3V	CLK0	AD[31]	GND
5	NC	NC	NC	RST#	GND	GNT0#	GND
4	NC	NC	NC	V(I/O)	INTP*	INTS*	GND
3	NC	INTA#	INTB#	INTC#	5V	INTD#	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	NC	TRST#	+12V	5V	GND

* The INTP and INTS signals are terminated to V(I/O) and not implemented on the CP307.

Table 2-15: 64-bit CompactPCI Bus Connector J2 Pinout (CP307 Front I/O Vers.)

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	NC	NC	NC	NC	NC	NC	GND
21	NC	CLK6	GND	RSV	RSV	RSV	GND
20	NC	CLK5	GND	RSV	RSV	RSV	GND
19	NC	GND	GND	RSV	RSV	RSV	GND
18	NC	RSV	RSV	RSV	RSV	RSV	GND
17	NC	RSV	RSV	PRST#	REQ6#	GNT6#	GND
16	NC	RSV	RSV	DEG#	RSV	RSV	GND
15	NC	RSV	RSV	FAL#	REQ5#	GNT5#	GND
14	NC	AD[35]	AD[34]	AD[33]	RSV	AD[32]	GND
13	NC	AD[38]	RSV	RSV	AD[37]	AD[36]	GND
12	NC	AD[42]	AD[41]	AD[40]	RSV	AD[39]	GND
11	NC	AD[45]	RSV	RSV	AD[44]	AD[43]	GND
10	NC	AD[49]	AD[48]	AD[47]	RSV	AD[46]	GND
9	NC	AD[52]	GND	RSV	AD[51]	AD[50]	GND
8	NC	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	NC	AD[59]	RSV	RSV	AD[58]	AD[57]	GND
6	NC	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	NC	C/BE[5]#	GND	RSV	C/BE[4]#	PAR64	GND
4	NC	V(I/O)	RSV	C/BE[7]#	RSV	C/BE[6]#	GND
3	NC	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	NC	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	NC	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Note ...

The 64-bit CompactPCI signals are not used on the board, but all 64 control and address signals are terminated to V(I/O).

2.3.7 Optional Rear I/O Interface

The CP307 board provides optional Rear I/O connectivity for special compact systems. Some standard PC interfaces are implemented and assigned to the front panel and to the rear connector J2.

When the Rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the Rear I/O module interface. Thus the Rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system Rear I/O feature a special backplane is necessary. The CP307 with Rear I/O is compatible with all standard CompactPCI passive backplanes with Rear I/O support on the system slot.

The CP307 Rear I/O provides the following interfaces (all signals are available on J2 only if the board is ordered with Rear I/O functionality):

- 32-bit/33 MHz CompactPCI (J1) and Rear I/O (J2)
- Two USB 2.0 ports
- Two Gigabit Ethernet ports without LED signals
- Two SATA ports
- Two COM ports (3.3 V TTL level)
- VGA analog port
- One fan control input
- One PWM output
- Management and control signals
- Input for +5V standby power

Note ...

The pinout of the Rear I/O connector is not compatible with that of the CP302, CP303, CP304, CP306, etc. For this reason, previously designed Rear I/O modules cannot be used with the CP307.

2.3.7.1 Optional Rear I/O Interface on CompactPCI Connector J2

Warning!

To support the Rear I/O feature a special backplane is necessary. Do not plug a Rear I/O configured board in a non-system slot Rear I/O backplane. Failure to comply with the above will result in damage to your board.

Table 2-16: Rear I/O CompactPCI Bus Connector J2 Pinout (CP307 Rear I/O Vers.)

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	NC	NC	NC	NC	NC	NC	GND
21	NC	CLK6	GND	USB1P / bi	USB3P / bi	USB1_5V / out	GND
20	NC	CLK5	GND	USB1N / bi	USB3N / bi	USB3_5V / out	GND
19	NC	GND	GND	PWR_BTN# / in	PWR_SLPS3# / out	RIO_3.3V / out	GND
18	NC	1RXD / in	1DCD / in	1DTR / out	GPI1/2CTS / in	1CTS / in	GND
17	NC	1TXD / out	GPI0/2RXD / in	PRST#	REQ6#	GNT6#	GND
16	NC	1DSR / in	1RTS / out	DEG#	RSV	1RI / in	GND
15	NC	PWR_5VSTDBY / in	FAN_SENSE / in	FAL#	REQ5#	GNT5#	GND
14	NC	IPA_DA+ / bi	IPA_DA- / bi	GPO1/2RTS / out	IPA_DC+ / bi	IPA_DC- / bi	GND
13	NC	IPA_DB+ / bi	IPA_DB- / bi	GPI4/2RI / in	IPA_DD+ / bi	IPA_DD- / bi	GND
12	NC	IPB_DA+ / bi	IPB_DA- / bi	RIO_2V5 / out	IPB_DC+ / bi	IPB_DC- / bi	GND
11	NC	IPB_DB+ / bi	IPB_DB- / bi	GPI3/2DCD / in	IPB_DD+ / bi	IPB_DD- / bi	GND
10	NC	NC	GPO0/2TXD / out	VGA_RED / out	GPO2/2DTR / out	NC	GND
9	NC	SATA3TXP / out	GND	VGA_HSYNC / out	NC	SATA1TXP / out	GND
8	NC	SATA3TXN / out	NC	VGA_BLUE / out	GND	SATA1TXN / out	GND
7	NC	NC	GPI2/2DSR / in	VGA_I2C_DAT / bi	PWM_OUT / out OD*	NC	GND
6	NC	SATA3RXP / in	NC	VGA_GREEN / out	GND	SATA1RXP / in	GND
5	NC	SATA3RXN / in	GND	VGA_VSYNC / out	NC	SATA1RXN / in	GND
4	NC	VI/O	RIO_5V / out	VGA_I2C_CLK / out	GPIO_CFG0 / in	NC	GND
3	NC	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	NC	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	NC	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

* Pin D7 is an open drain output and has no pull-up resistor on the CP307.

Warning!

The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

Note ...

The signal on the GPIO configuration pin D4 tolerates only 3.3 V signalling and has an internal pull-up resistor to 3.3V.

The pins for the interfaces COM1 and GPIO/COM2 (pins A18, A17, A16, B18, B17, B16, B10, B7, C18, C14, C13, C11, D18, D10, E18, and E16) tolerate only 3.3 V signaling and their inputs have internal pull-up resistors.

Legend for Table 2-15:

SATAx	Serial ATA port
IPx	Gigabit Ethernet port
USBx	USB interface and power
VGAx	VGA signals
COM1x	COM1 port
GPIOx	COM2 port or GPIO
PWRx	Power Management signals
5V/3.3V	Power
GPIO_CFG0	GPIO configuration (GPIO or COM2)

With the GPIO_CFG0 signal on the Rear I/O module the active interface can be selected.

Table 2-17: GPIO Signal Description

GPIO SIGNAL	DESCRIPTION
GPIO_CFG0	0: COM1; GPIO 1: COM1; COM2

Note ...

The default value is 1 if the pin is not connected (pull-up resistor on CP307). If connected, the default value is depending on the Rear I/O module.

2.3.7.2 Rear I/O Configuration

Rear I/O interfaces are only available on Rear I/O versions of the board.

In order to implement the system Rear I/O feature, a system slot Rear I/O backplane is necessary. This backplane must comply with the CompactPCI Specification PICMG 2.0 R3.0, October 1999.

Warning!

To support the Rear I/O feature a special backplane is necessary. Do not plug a Rear I/O configured board in a non-system slot Rear I/O backplane. This will damage the board.

Ethernet Interfaces

Gigabit Ethernet signals are available either on the front RJ-45 connector or on the Rear I/O interface due the implemented switches on the CP307.

Both Gigabit Ethernet channels are individually switchable to front or Rear I/O. Switching over from front to Rear I/O or vice versa is effected using the BIOS settings or the board-specific registers (default: front I/O). For further information on the BIOS settings, refer to the CP307 BIOS Guide, Chapter 8, OEM Feature. For further information on the board-specific registers, refer to chapter 4.5.5, Table 4-10, “I/O Configuration Register”.

VGA Interface

VGA signals are available either on the front VGA connector, J6, or on the Rear I/O interface due the implemented switches on the CP307. Switching over from front to Rear I/O or vice versa is effected using the BIOS (default: front I/O).

Note ...

The CP307 provides 150 Ω termination resistors for the red, green and blue VGA signals.

Thus, further 150 Ω termination resistors are necessary on the Rear I/O module to reach the required 75 Ω termination for the VGA connection.

Serial Interface COM1 and COM2

The COM1 is available either on the front panel of the 8HP CP307 version or on the Rear I/O interface. Switching over from front to Rear I/O or vice versa is effected using the BIOS settings or the board-specific registers (default: front I/O). For further information refer to chapter 4.5.5, Table 4-10, “I/O Configuration Register”.

The COM2 port can be used only on the Rear I/O interface.

USB Interface

There are six independent USB interfaces available, four ports are routed to the 4-pin front I/O connectors (two on the 4HP CP307 version and two further on the 8HP CP307 version). The other two ports are only available on the Rear I/O connector.

Note ...

All six USB ports may be used at the same time. It is strongly recommended to use cables less than 3 metres in length for the Rear I/O interfaces.

SATA Interface

The CP307 provides up to four SATA interfaces. Two SATA ports, SATA1 and SATA3, can be used only on the Rear I/O interface. All SATA ports can be used simultaneously.

Table 2-18: SATA Port Features

SATA PORT	CONNECTOR	USAGE	AVAILABLE WITH
SATA0	J4 on the CP307 baseboard	external SATA HDD drives, e.g. 2.5” or 3.5 SATA HDDs	CP307 4HP and 8HP front and rear I/O board versions
SATA1	J6 on the CP-RIO3-04 Rear I/O module	external SATA HDD drives, e.g. 2.5” or 3.5 SATA HDDs	CP307 4HP and 8HP rear I/O board versions
SATA2	J5 on the CP307-HDD module (8HP)	onboard 2.5” SATA HDD drive mounted on CP307-HDD module	CP307 8HP front and rear I/O board versions
SATA3	J5 on the CP-RIO3-04 Rear I/O module	external SATA HDD drives, e.g. 2.5” or 3.5 SATA HDDs	CP307 4HP and 8HP rear I/O board versions

Chapter 3

Installation

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3. Installation

The CP307 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the CP307. *Kontron* assumes no responsibility for any damage resulting from failure to comply with these requirements.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

Caution!

If your board type is not specifically qualified as being hot swap capable, switch off the CompactPCI system power before installing the board in a free CompactPCI slot. Failure to do so could endanger your life or health and may damage your board or system.

Note ...

Certain CompactPCI boards require bus master and/or Rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

ESD Equipment!

This CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

3.2 CP307 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the CP307 in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of the CP307 in a system proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed.

   Warning!

   Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the CP307 refer to Chapter 4. For the installation of CP307-specific peripheral devices and Rear I/O devices refer to the appropriate sections in Chapter 3.

   Warning!

   Care must be taken when applying the procedures below to ensure that neither the CP307 nor other system boards are physically damaged by the application of these procedures.

3. To install the CP307 perform the following:
   1. Ensure that no power is applied to the system before proceeding.

      Warning!

      When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
   3. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
   4. Fasten the front panel retaining screws (two on the 4HP version and four on the 8HP).
   5. Connect all external interfacing cables to the board as required.
   6. Ensure that the board and all required interfacing cables are properly secured.

The CP307 is now ready for operation. For operation of the CP307, refer to the appropriate CP307-specific software, application, and system documentation.

3.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP307 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws (two on the 4HP version and four on the 8HP).
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

3.4 Hot Swap Procedures

The CP307 is not designed for hot swap operation. Do not attempt to hot swap this board. However, the CP307 supports the addition or removal of other boards whilst in a powered-up state.

3.5 Installation of CP307 Peripheral Devices

The CP307 is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following chapters provide information regarding installation aspects and not detailed procedures.

3.5.1 CompactFlash Installation

The CompactFlash socket supports all available CompactFlash ATA cards type I and type II.

Note ...

The CP307 does not support removal and reinsertion of the CompactFlash storage card while the board is in a powered-up state. Connecting the CompactFlash cards while the power is on, which is known as "hot plugging", may damage your system.

3.5.2 USB Device Installation

The CP307 supports all USB plug and play computer peripherals (e.g. keyboard, mouse, printer, etc.).

Note ...

All USB devices may be connected or removed while the host or other peripherals are powered up.

3.5.3 Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery type is CR2025.

Note ...

The user must be aware that the battery's operational temperature range is less than the CP307's storage temperature range.

For exact range information, refer to the battery manufacturer's specifications.

Note ...

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

The typical life expectancy of a 170 mAh battery (CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 4 - 5 years.

Note ...

If a CP307-HDD module is used on the CP307, either the CP307 or the CP307-HDD module may be equipped with a battery.

Using one battery on the CP307 and one on the CP307-HDD module simultaneously may result in premature discharge of the batteries.

3.5.4 Hard Disk Installation

The following information pertains to hard disks which may be connected to the CP307 via SATA or IDE cabling. To install a hard disk, it is necessary to perform the following operations in the given order:

1. Install the hardware.

Warning!

The incorrect connection of power or data cables may damage your hard disk unit and/or the CP307 board.

Note ...

Some symptoms of incorrectly installed HDDs are:

- Hard disk drives are not auto-detected: may be a master/slave problem (only for IDE HDD) or a bad SATA or IDE cable. Should this occur, contact your vendor.
- Hard Disk Drive fail message at boot-up: may be a bad cable or lack of power going to the drive.
- No video on boot-up: usually means the cable is installed backwards (can only occur if not-coded cables are used).
- Hard drive light is constantly on: usually means bad cable or defective drives/ motherboard. Should this occur, try another HDD.
- Hard drives do not power up: check power cables and cabling. This may also result from a bad power supply or HDD drive.

2. Initialize the software necessary to run the chosen operating system.

3.6 Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to the appropriate OS software documentation for installation.

Note ...

Users working with pre-configured operating system installation images for Plug and Play compliant operating systems, for example Windows® XP, Windows® XP Embedded, must take into consideration that the stepping and revision ID of the chipset and/or other onboard PCI devices may change. Thus, a re-configuration of the operating system installation image deployed for a previous chipset stepping or revision ID is in most cases required. The corresponding operating system will detect new devices according to the Plug and Play configuration rules.

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Chapter 4

Configuration

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4. Configuration

4.1 Clearing BIOS CMOS Setup

If the system does not boot (due to, for example, the wrong BIOS configuration or wrong password setting), the CMOS setting may be cleared using the solder jumper JP1.

Procedure for clearing the CMOS setting:

The system is booted with the jumper in the new, closed position, then powered down again. The jumper is reset back to the normal position, then the system is rebooted again.

Table 4-1: Clearing BIOS CMOS Setup

JP1	DESCRIPTION
Open	***Normal boot using the CMOS settings***
Closed	Clear the CMOS settings and use the default values

The default setting is indicated by using italic bold.

4.2 Legacy Interrupts

The CP307 board uses the standard AT IRQ routing (8259 controller) for legacy devices.

The following table indicates the default interrupt routing. The shaded table cells indicate the interrupt routings which can be modified or disabled via the BIOS setup.

Table 4-2: Legacy Interrupt Setting

IRQ	PRIORITY	STANDARD FUNCTION
IRQ0	1	System Timer
IRQ1	2	Keyboard Controller
IRQ2	--	Input of the second IRQ controller (IRQ8-IRQ15)
IRQ3	11	COM2
IRQ4	12	COM1
IRQ5	13	Watchdog
IRQ6	14	Free
IRQ7	15	Free
IRQ8	3	System Real-Time Clock
IRQ9	4	APIC
IRQ10	5	Free
IRQ11	6	Free
IRQ12	7	PS/2 mouse: on the 8HP version Free: on the 4HP version
IRQ13	8	Coprocessor error
IRQ14	9	IDE/CompactFlash/SATA
IRQ15	10	Free
NMI		Watchdog

Warning!

IRQ5 should normally have only **one** source enabled, otherwise improper system operation may result.

If more than one source is required to be enabled, please contact Kontron before implementing the IRQs.

For events that are not time critical, such as ENUM, DERATE, etc., polling should be considered instead of using an IRQ.

4.3 Onboard PCI Interrupt Routing

The ICH7-R provides up to eight PCI interrupt inputs. The table below describes the connection of these IRQ signals.

Table 4-3: PCI Interrupt Routing

ICH7-R IRQ INPUT	CPCI INTERFACE	FUNCTION INTERNAL ICH7-R
PIRQA	Not available	USB EHCI Controller IDE USB UHCI 0 Controller PCI Express 1 (Gigabit Ethernet 1)
PIRQB	Not available	SMBUS SATA USB UHCI 1 Controller PCI Express 2 (Gigabit Ethernet 2)
PIRQC	Not available	USB UHCI 2 Controller
PIRQD	Not available	USB UHCI 3 Controller
PIRQE	CPCI INTA	Not used
PIRQF	CPCI INTB	Not used
PIRQG	CPCI INTC	Not used
PIRQH	CPCI INTD	Not used

For more information, refer to the INTEL ICH7-R data sheet.

4.4 Memory Map

The CP307 board uses the standard AT ISA memory map.

4.4.1 Memory Map for the 1st Megabyte

The following table sets out the memory map for the first megabyte:

Table 4-4: Memory Map for the 1st Megabyte

MEMORY RANGE	SIZE	FUNCTION
0xE0000 – 0xFFFFF	128 k	BIOS implemented in FWH Reset vector 0xFFFF0
0xD0000 – 0xDFFFF	64 k	Free
0xCF000 – 0xCFFFF	4 k	Free
0xC0000 – 0xCEFFF	60 k	VGA BIOS
0xA0000 – 0xBFFFF	128 k	Normally used as video RAM as follows: CGA video: 0xB8000-0xBFFFF Monochrome video: 0xB0000-0xB7FFF EGA/VGA video: 0xA0000-0xAFFFF
0x000000 – 0x9FFFF	640 k	DOS reserved memory space

4.4.2 I/O Address Map

The following table sets out the memory map for the I/O memory. The shaded table cells indicate CP307-specific registers.

Table 4-5: I/O Address Map

ADDRESS	DEVICE
0x000 - 0x00F	DMA Controller #1
0x020 - 0x021	Interrupt Controller #1
0x022 - 0x02D	Reserved
0x02E - 0x02F	Super I/O
0x040 - 0x043	Timer
0x060 - 0x063	Keyboard Interface
0x070 - 0x071	RTC Port
0x080	BIOS POST Code
0x081 - 0x08F	DMA Page Register
0x0A0 - 0x0B0	Interrupt Controller #2
0x0C0 - 0x0DF	DMA Controller #2
0x0E0 - 0x0EF	Reserved
0x0F0 - 0x0FF	Math Coprocessor
0x170 - 0x17F	Hard Disk Secondary
0x1F0 - 0x1FF	Hard Disk Primary
0x19C - 0x19F	Reserved
0x280	Reserved
0x281	Reserved
0x282	Watchdog Timer Control Register
0x283	Reserved
0x284	Hardware and Logic Revision Index Register
0x285	Reset Status Register
0x286	I/O Status Register
0x287	I/O Configuration Register
0x288	Board ID Register
0x289	Board Interrupt Configuration Register
0x28A - 0x28C	Reserved
0x28D	LED Control Register
0x28E	Rear I/O GPIO Register
0x28F	Delay Timer Control/Status Register
0x2F8 - 0x2FF	Serial Port COM2
0x378 - 0x37F	Reserved
0x3F0 - 0x3F7	Reserved
0x3F8 - 0x3FF	Serial Port COM1
0xCA2 - 0xCA5	Reserved
0xA00 - 0xAFF	Super I/O Power Management Register

4.5 CP307-Specific Registers

The following registers are special registers which the CP307 uses to watch the onboard hardware special features and a number of CompactPCI control signals.

Normally, only the system BIOS uses these registers, but they are documented here for application use as required.

Note ...
Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

4.5.1 Watchdog Timer Control Register

The CP307 has one Watchdog Timer provided with a programmable timeout ranging from 125 msec to 256 sec. Failure to strobe the Watchdog Timer within a set time period results in a system reset, NMI or an interrupt. The NMI and interrupt mode can be configured via the board interrupt configuration register (0x289).

There are four possible modes of operation involving the Watchdog Timer:

- Timer only mode
- Reset mode
- Interrupt mode
- Dual stage mode

At power on the Watchdog is not enabled. If not required, it is not necessary to enable it. If required, the bits of the Watchdog Timer Control Register (0x282) must be set according to the application requirements. To operate the Watchdog, the mode and time period required must first be set and then the Watchdog enabled. Once enabled, the Watchdog can only be disabled or the mode or the timeout changed by powering down and then up again. To prevent a Watchdog timeout, the Watchdog must be retriggered before timing out. This is done by writing a ’1’ to the WTR bit. In the event a Watchdog timeout does occur, the WTE bit is set to ’1’. What transpires after this depends on the mode selected.

The four operational Watchdog Timer modes can be configured by the WMD[1:0] bits, and are described as follows:

Timer only mode - In this mode the Watchdog is enabled using the required timeout period. Normally, the Watchdog is retriggered by writing a ’1’ to the WTR bit. In the event a timeout occurs, the WTE bit is set to ’1’. This bit can then be polled by the application and handled accordingly. To continue using the Watchdog, write a ’1’ to the WTE bit, and then retrigger the Watchdog using WTR. The WTE bit retains its setting as long as no power down-up is done. Therefore, this bit may be used to verify the status of the Watchdog.

Reset mode - This mode is used to force a hard reset in the event of a Watchdog timeout. To be effective, the hard reset must not be masked or otherwise negated. In addition, the WTE bit is not reset by the hard reset, which makes it available if necessary to determine the status of the Watchdog prior to the reset.

Interrupt mode - This mode causes the generation of an interrupt in the event of a Watchdog timeout. The interrupt handling is a function of the application. If required, the WTE bit can be used to determine if a Watchdog timeout has occurred.

Dual stage mode - This is a complex mode where in the event of a timeout two things occur: 1) an interrupt is generated, and 2) the Watchdog is retriggered automatically. In the event a second timeout occurs immediately following the first timeout, a hard reset will be generated. If the

Watchdog is retriggered normally, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the other modes, the WTE bit is available for application use.

Table 4-6: Watchdog Timer Control Register

REGISTER NAME		WATCHDOG TIMER CONTROL REGISTER						SIZE	
ADDRESS		0x282						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WTE	WMD1	WMD0	WEN/WTR	WTM3	WTM2	WTM1	WTM0
DEFAULT		0	0	0	0	0	0	0	0
ACCESS		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT	NAME	DESCRIPTION / FUNCTION							
7	WTE	Watchdog Timer Expired status bit: 0 Watchdog Timer has not expired 1 Watchdog Timer has expired Writing a '1' to this bit resets it to 0							
6 - 5	WMD[1:0]	Watchdog mode settings: **WMD1 WMD0 Mode** 0 0 Timer only 0 1 Reset 1 0 Interrupt 1 1 Dual Stage							
4	WEN/WTR	Watchdog enable / watchdog trigger control bit: 0 Watchdog Timer has not been enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog Timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog Timer is enabled, it will indicate a '1'. 1 Watchdog Timer is enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3:0].							
3 - 0	WTM[3:0]	Watchdog timeout time settings: **WTM3 WTM2 WTM1 WTM0 Value** 0 0 0 0 125 ms 0 0 0 1 250 ms 0 0 1 0 500 ms 0 0 1 1 1 s 0 1 0 0 2 s 0 1 0 1 4 s 0 1 1 0 8 s 0 1 1 1 16 s 1 0 0 0 32 s 1 0 0 1 64 s 1 0 1 0 128 s 1 0 1 1 256 s 1 1 0 0 reserved 1 1 0 1 reserved 1 1 1 0 reserved 1 1 1 1 reserved The nominal timeout period is 5% longer than the above-stated values.							

4.5.2 Hardware and Logic Revision Index Register

The Hardware and Logic Revision Index Register signals to the software when differences in the hardware and the logic require different handling by the software. It starts with the value 0x00 for the initial board prototypes and will be incremented with each change in hardware as development continues.

Table 4-7: Hardware and Logic Revision Index Register

REGISTER NAME	HARDWARE AND LOGIC REVISION INDEX REGISTER						SIZE	
ADDRESS	0x284						8 bits	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	HWRI3	HWRI2	HWRI1	HWRI0	LRI3	LRI2	LRI1	LRI0
DEFAULT	0	0	0	0	0	0	0	0
ACCESS	R	R	R	R	R	R	R	R

BIT	NAME	DESCRIPTION / FUNCTION
7 - 4	HWRI[3:0]	Hardware revision ID: 0000 Index 0000
3 - 0	LRI[3:0]	Logic revision ID: 0000 Index 0000

4.5.3 Reset Status Register

The Reset Status Register is used to determine the reset source. The I/O location is 0x285.

Table 4-8: Reset Status Register

REGISTER NAME	RESET STATUS REGISTER						SIZE	
ADDRESS	0x285						8 bits	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	PRST	Res.	Res.	Res.	Res.	FRST	Res.	WRST
DEFAULT	0	0	0	0	0	0	0	0
ACCESS	R/W	R	R	R	R	R/W	R	R/W

BIT	NAME	DESCRIPTION / FUNCTION
7	PRST*	0 Indicates the state after setting back the bit 1 Power-on reset (cold start)
6 - 3	Res.	Reserved
2	FRST*	0 System reset generated by power-on reset 1 System reset generated by front panel reset
1	Res.	Reserved
0	WRST*	0 System reset generated by power-on reset 1 System reset generated by Watchdog

* Read/Write Clear. Writing a ’1’ to this bit clears the bit.

Note ...

The Reset Status Register is set to the default values by power-on reset, not by PCI reset.

4.5.4 I/O Status Register

The I/O Status Register describes the CompactPCI, the Rear I/O and the local control signals. The Rear I/O configuration is shown by the bits RCFG[1:0]. To indicate the active Firmware Hub, the FSTA[1:0] bits are used. The CSLOT bit reflects the kind of slot in which the CP307 is plugged in. The fail signal is an output of the power supply and indicates a power supply failure. For the description of the derate and enumeration signals, please refer to the Board Interrupt Configuration Register (0x289).

Table 4-9: I/O Status Register

REGISTER NAME	I/O STATUS REGISTER						SIZE	
ADDRESS	0x286						8 bits	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	RCFG1	RCFG0	FSTA1	FSTA0	CSLOT	CENUM	CFAIL	CDER
DEFAULT	--	--	0	0	0	0	0	0
ACCESS	R	R	R	R	R	R	R	R

BIT	NAME	DESCRIPTION/FUNCTION
7 - 6	RCFG[1:0]	These bits indicate the Rear I/O configuration: 00 Rear I/O disabled 01 COM1, GPIO 10 Reserved 11 COM1, COM2 The default value of these bits depends on the CP307 version ordered (front or rear I/O) and on the Rear I/O module, if used.
5 - 4	FSTA[1:0]	These bits indicate the active BIOS Firmware Hub Flash status: 00 BIOS boot from FWH0 01 Reserved 10 BIOS boot from external FWH on the CP307-HDD module 11 Reserved
3	CSLOT	0 Installed in a system slot 1 Installed in a peripheral slot
2	CENUM	0 Indicates the insertion or removal of a hot swap system board (CPCI ENUM) 1 No hot swap event
1	CFAIL	0 Power supply failure (CPCI FAIL signal) 1 Power normal
0	CDER	0 Power derating (CPCI DEG signal) 1 Power normal

4.5.5 I/O Configuration Register

The I/O Configuration Register holds a series of bits defining the onboard configuration.

Table 4-10: I/O Configuration Register

REGISTER NAME	I/O CONFIGURATION REGISTER							SIZE
ADDRESS	0x287							8 bits
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	Res.	POST	LED1	LED0	BBEI	SCOM1	SETH2	SETH1
DEFAULT	0	0*	0	0	0*	1	0	0
ACCESS	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

BIT	NAME	DESCRIPTION / FUNCTION
7	Res.	Reserved
6	POST	POST LEDs' configuration: 0 Enabled 1 Disabled
5	LED1	LED1 configuration/enable: 0 Overtemperature LED 1 General Purpose LED
4	LED0	LED0 configuration/enable: 0 Watchdog LED 1 General Purpose LED
3	BBEI	BIOS Boot End Indication: 0 BIOS is booting 1 BIOS boot finished
2	SCOM1	COM1 routing selection: 0 Rear I/O 1 CP307-HDD module
1	SETH2	Ethernet 2 routing selection: 0 Front I/O 1 Rear I/O
0	SETH1	Gigabit Ethernet 1 routing selection: 0 Front I/O 1 Rear I/O

* The default settings of bits 6 and 3 change during the BIOS boot. After bit 3 is set, it can only be cleared by a board reset.

4.5.6 Board ID Register

This register describes the hardware and the board index. The content of this register is unique for each Kontron board.

Table 4-11: Board ID Register

REGISTER NAME		BOARD ID REGISTER						SIZE	
ADDRESS		0x288						8 bits	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		BID7	BID6	BID5	BID4	BID3	BID2	BID1	BID0
DEFAULT		1	0	1	0	1	0	0	0
ACCESS		R	R	R	R	R	R	R	R
BIT	NAME	DESCRIPTION / FUNCTION							
7 - 0	BID[7:0]	Board ID: 0xA8 CP307 / CP307-V							

4.5.7 Board Interrupt Configuration Register

The Board Interrupt Configuration register holds a series of bits defining the interrupt routing for the Watchdog. If the Watchdog Timer fails, it can generate two independent hardware events: NMI and IRQ5 interrupt.

The enumeration signal is generated by a hot swap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board. The derate signal indicates that the power supply is beginning to derate its power output.

Table 4-12: Board Interrupt Configuration Register

REGISTER NAME	BOARD INTERRUPT CONFIGURATION REGISTER						SIZE	
ADDRESS	0x289						8 bits	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	Res.	CFNMI	CFIRQ	CEIRQ	CDIRQ	Res.	WIRQ1	WIRQ0
DEFAULT	0	0	0	0	0	0	0	0
ACCESS	R	R/W	R/W	R/W	R/W	R	R/W	R/W

BIT	NAME	DESCRIPTION / FUNCTION
7	Res.	Reserved
6	CFNMI	CPCI fail signal to NMI routing: 0 Disabled 1 Enabled
5	CFIRQ	CPCI fail signal to IRQ5 routing: 0 Disabled 1 Enabled
4	CEIRQ	CPCI enum signal to IRQ5 routing: 0 Disabled 1 Enabled
3	CDIRQ	CPCI derate signal to IRQ5 routing: 0 Disabled 1 Enabled
2	Res.	Reserved
1 - 0	WIRQ[1:0]	Watchdog interrupt routing: 11 NMI 10 Reserved 01 IRQ5 00 Disabled

4.5.8 LED Control Register

The LED Control Register enables the user to switch on and off the General Purpose LEDs on the front panel.

Table 4-13: LED Control Register

REGISTER NAME	LED CONTROL REGISTER						SIZE	
ADDRESS	0x28D						8 bits	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	Res.	Res.	Res.	Res.	Res.	Res.	LED1	LED0
DEFAULT	0	0	0	0	0	0	0	0
ACCESS	R	R	R	R	R	R	R/W	R/W

BIT	NAME	DESCRIPTION / FUNCTION
7 - 2	Res.	Reserved
1	LED1	LED1 (TH/GP) control settings: 0 LED off 1 LED on
0	LED0	LED0 (WD/GP) control settings: 0 LED off 1 LED on

4.5.9 Rear I/O GPIO Register

The Rear I/O GPIO Register controls the General Purpose outputs and holds the status of the General Purpose inputs. This register can only be used if the Rear I/O configuration bits RCFG[1:0] in Table 4-9 are set to “01” (i.e. if the GPIO function is enabled).

Table 4-14: Rear I/O GPIO Register

REGISTER NAME	REAR I/O GPIO REGISTER						SIZE	
ADDRESS	0x28E						8 bits	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	GPO2	GPO1	GPO0	GPI4	GPI3	GPI2	GPI1	GPI0
DEFAULT	0	0	0	1	1	1	1	1
ACCESS	R/W	R/W	R/W	R	R	R	R	R

BIT	NAME	DESCRIPTION / FUNCTION
7	GPO2	GPO2 signal (3.3V TTL): 0 Output low 1 Output high
6	GPO1	GPO1 signal (3.3V TTL): 0 Output low 1 Output high
5	GPO0	GPO0 signal (3.3V TTL): 0 Output low 1 Output high
4	GPI4	GPI4 signal (3.3V TTL): 0 Input low 1 Input high
3	GPI3	GPI3 signal (3.3V TTL): 0 Input low 1 Input high
2	GPI2	GPI2 signal (3.3V TTL): 0 Input low 1 Input high
1	GPI1	GPI1 signal (3.3V TTL): 0 Input low 1 Input high
0	GPI0	GPI0 signal (3.3V TTL): 0 Input low 1 Input high

Note ...

The CP307 provides pull-up resistors on the Rear I/O signal pins GPI[4:0] which leads to the default setting “input high” if the inputs are not connected.

The General Purpose Inputs support 3.3V TTL signalling only.

4.5.10 Delay Timer Control/Status Register

The delay timer enables the user to realize short, reliable delay times. It runs by default and does not start again on its own. It can be restarted at anytime by writing anything other than a '0' to the delay timer control/status register. The hardware delay timer provides a set of outputs for defined elapsed time periods. The timer outputs reflected in the Delay Timer Control/Status Register are set consecutively and remain set until the next restart is triggered again.

Table 4-15: Delay Timer Control/Status Register

REGISTER NAME	DELAY TIMER CONTROL/STATUS REGISTER						SIZE	
ADDRESS	0x28F						8 bits	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	DTC7	DTC6	DTC5	DTC4	DTC3	DTC2	DTC1	DTC0
DEFAULT	0	0	0	0	0	0	0	0
ACCESS	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	NAME	DESCRIPTION/FUNCTION
7 - 0	DTC[7:0]	The hardware delay timer is operated via one simple 8-bit control/status register. During normal operation, each of the 8 bits reflects a timer output which means defined elapsed time period after the last restart according to the following bit mapping: **DTC[7:0] Value Accuracy** Bit 7: 1 ms < + 0.04% Bit 6: 500 µs < + 0.08% Bit 5: 250 µs < + 0.16% Bit 4: 100 µs < + 0.4% Bit 3: 50 µs < + 0.8% Bit 2: 10 µs < + 4% Bit 1: 5 µs < + 8% Bit 0: 1 µs < + 40%

Since the timer width and thus the availability of outputs varies over different implementations, it is necessary to be able to determine the timer capability. Therefore, writing a '0' to the Delay Timer Control/Status Register followed by reading indicates the timer capability (not the timer outputs). For example, writing 0x00 and then reading 0xFF results in a 8-bit wide timer register. This status register mode can be switched off to normal timer operation by writing anything other than a '0' to this register.

Chapter 5

Power Considerations

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5. Power Considerations

5.1 System Power

The considerations presented in the ensuing chapters must be taken into account by system integrators when specifying the CP307 system environment.

5.1.1 CP307 Baseboard

The CP307 baseboard itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the CP307 should be carefully tested to ensure compliance with these ratings.

Table 5-1: Maximum Input Power Voltage Limits

SUPPLY VOLTAGE	MAXIMUM PERMITTED VOLTAGE
+3.3 V	+3.6 V
+5 V	+5.5 V

Warning!

The maximum permitted voltages indicated in the table above must not be exceeded. Failure to comply with the above may result in damage to your board.

The following table specifies the ranges for the different input power voltages within which the board is functional. The CP307 is not guaranteed to function if the board is operated beyond the prescribed limits.

Table 5-2: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE
+3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.
+5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.

5.1.2 Backplane

Backplanes to be used with the CP307 must be adequately specified. The backplane must provide optimal power distribution for the +3.3 V, +5 V and +12 V power inputs. It is recommended to use only backplanes which have at least two power planes for the +3.3 V and +5 V voltages.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use POSITRONIC or M-type connector backplanes and power supplies where possible.

5.1.3 Power Supply Units

Power supplies for the CP307 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the CP307 has been optimized for minimal power consumption, the power supply unit must be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane.

Note ...

Non-industrial ATX PSUs may require a greater minimum load than a single CP307 is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP307 may hangup. The solution is to use an industrial PSU or to add more load to the system.

The start-up behavior of CPCI and PCI (ATX) power supplies is critical for all new CPU boards. These boards require a defined power sequence and start-up behavior of the power supply. For information on the required behavior refer to the power supply specifications on the formfactors.org web site and to the CompactPCI (PICMG) specification on the picmgeu.org web site.

5.1.3.1 Start-Up Requirement

Power supplies must comply with the following guidelines, in order to be used with the CP307.

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

5.1.3.2 Power-Up Sequence

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation.

Both voltages must reach their minimum in-regulation level not later than 20 ms after the output power ramp start.

5.1.3.3 Tolerance

The tolerance of the voltage lines is described in the CPCI specification (PICMG 2.0 R3.0).The recommended measurement point for the voltage is the CPCI connector on the CPU board.

The following table provides information regarding the required characteristics for each board input voltage.

Table 5-3: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)	REMARKS
5 V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
3.3 V	+3.3 VDC	+5%/-3%	50 mV	Main voltage
+12 V	+12 VDC	+5%/-5%	240 mV	Not required
-12 V	-12 VDC	+5%/-5%	240 mV	Not required
V I/O (PCI) signalling voltage	+3.3 VDC or +5 VDC	+5%/-3%	50 mV	depends on board version
GND	Ground, not directly connected to potential earth (PE)			

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

5.1.3.4 Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Warning!

All of the input voltages must be functionally coupled to each other so that if one input voltage fails, all other input voltages must be regulated proportionately to the failed voltage. For example, if the +5V begins to decrease, all other input voltages must decrease accordingly. This is required in order to preclude cross currents within the CP307.

Failure to comply with above may result in damage to the board or improper system operation.

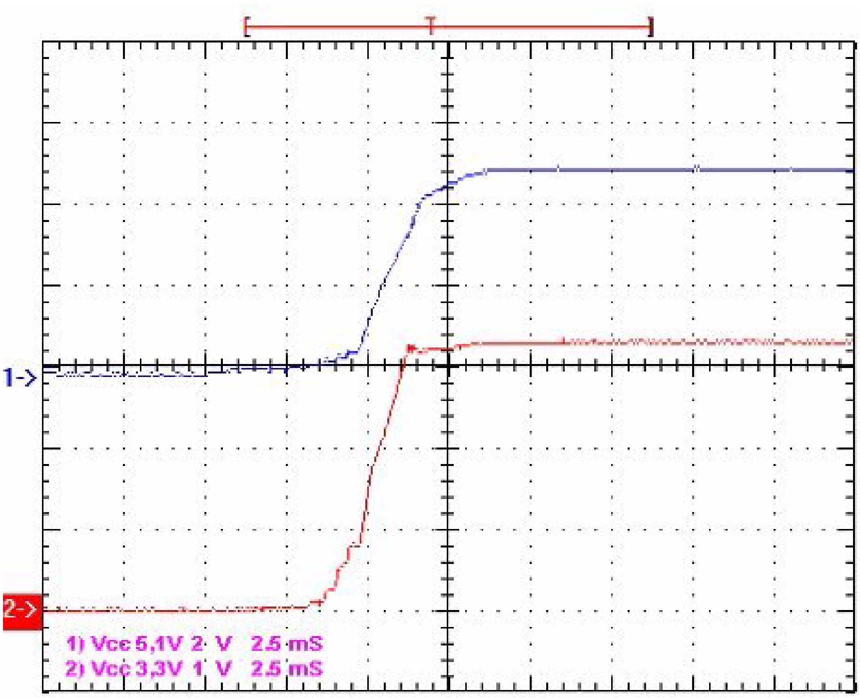
Note ...

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.1.3.5 Rise Time Diagram

The following figure illustrates an example of the recommended start-up ramp of a CPCI power supply for all Kontron boards delivered up to now.

Figure 5-1: Start-Up Ramp of the CP3-SVE180 AC Power Supply



5.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the CP307 baseboard and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption tables below list the voltage and power specifications for the CP307 board and the CP307 accessories. The values were measured using an 8-slot passive CompactPCI backplane with two power supplies: one for the CP307 (5V and 3.3V power supply), and the other for the hard disk. The operating systems used were DOS, Linux and Windows® XP. All measurements were conducted at a temperature of 25°C. The measured values varied, because the power consumption was dependent on processor activity.

Note ...

The power consumption values indicated in the tables below can vary depending on the ambient temperature or the system performance. This can result in deviations of the power consumption values of up to 10%.

For the power consumption measurements, the CP307 was populated with the following processors:

- Intel® Core™ Duo processor U2500 (ULV), 1.2 GHz, 533 MHz FSB, 2 MB L2 cache
- Intel® Core™ Duo processor L2400 (LV), 1.66 GHz, 667 MHz FSB, 2 MB L2 cache
- Intel® Core™ Duo processor T2500 (SV), 2.0 GHz, 667 MHz FSB, 2 MB L2 cache
- Intel® Core™2 Duo processor L7400 (LV), 1.5 GHz, 667 MHz FSB, 4 MB L2 cache
- Intel® Core™2 Duo processor T7400 (SV), 2.16 GHz, 667 MHz FSB, 4 MB L2 cache

In addition, the following testing conditions were present during the power consumption measurements:

- DOS
  With this operating system only one processor core was active. This operating system has no power management support and provides a very simple method to verify the measured power consumption values.
- Linux/Windows® XP, IDLE Mode
  With these operating systems both processor cores were in IDLE state.

and under the following testing conditions:

- CP307 Thermal Design Power (TDP) at 75%
  These values represent the "typical" maximum power dissipation reached under OS-controlled applications.
- CP307 Thermal Design Power (TDP) at 100%
  These values represent the maximum power dissipation achieved through the use of specific tools to heat up the processor cores. 100% TDP is unlikely to be reached in real applications.

The following tables indicate the power consumption with soldered DDR2 SDRAM (there was no SODIMM memory module mounted on the CP307). For measurements made with the Linux and Windows® XP operating systems, the VGA resolution was 1024 x 768 pixels.

Table 5-4: Power Consumption: CP307 with DOS

POWER	CORE™ Duo 1.2 GHz (ULV)	CORE™ DUO 1.66 GHz (LV)	CORE™ DUO 2.0 GHz (SV)	CORE™2 DUO 1.5 GHz (LV)	CORE™2 DUO 2.16 GHz (SV)
5 V	8.7 W	12.0 W	19.7 W	12.0 W	20.7 W
3.3 V	3.2 W	3.1 W	3.1 W	3.1 W	3.1 W
Total	11.9 W	15.1 W	22.8 W	15.1 W	23.8 W

Table 5-5: Power Consumption: CP307 with Linux / Win.® XP in IDLE Mode

POWER	CORE™ Duo 1.2 GHz (ULV)	CORE™ DUO 1.66 GHz (LV)	CORE™ DUO 2.0 GHz (SV)	CORE™2 DUO 1.5 GHz (LV)	CORE™2 DUO 2.16 GHz (SV)
5 V	5.9 W	7.7 W	12.0 W	7.7 W	12.4 W
3.3 V	3.0 W	2.8 W	2.8 W	2.8 W	2.8 W
Total	8.9 W	10.5 W	14.8 W	10.5 W	15.2 W

Table 5-6: Power Consumption: CP307 TDP at 75%

POWER	CORE™ Duo 1.2 GHz (ULV)	CORE™ DUO 1.66 GHz (LV)	CORE™ DUO 2.0 GHz (SV)	CORE™2 DUO 1.5 GHz (LV)	CORE™2 DUO 2.16 GHz (SV)
5 V	9.4 W	14.7 W	30.0 W	16.9 W	31.3 W
3.3 V	3.4 W	3.0 W	3.1 W	3.0 W	3.0 W
Total	12.8 W	17.7 W	33.1 W	19.9 W	34.3 W

Table 5-7: Power Consumption: CP307 TDP at 100%

POWER	CORE™ Duo 1.2 GHz (ULV)	CORE™ DUO 1.66 GHz (LV)	CORE™ DUO 2.0 GHz (SV)	CORE™2 DUO 1.5 GHz (LV)	CORE™2 DUO 2.16 GHz (SV)
5 V	11.6 W	18.1 W	37.5 W	20.4 W	38.3 W
3.3 V	3.4 W	3.0 W	3.1 W	3.0 W	3.0 W
Total	15.0 W	21.1 W	40.6 W	23.4 W	41.3 W

5.3 Power Consumption of CP307 Accessories

The following table indicates the power consumption of the CP307 accessories.

Table 5-8: Power Consumption of CP307 Accessories

MODULE	POWER 5 V	POWER 3.3 V AVERAGE
DDR2 SDRAM SODIMM PC2 5300 CL5 (DDR2 667) 512 MB	—	1 W - 2 W
DDR2 SDRAM SODIMM PC2 5300 CL5 (DDR2 667) 1 GB	—	1 W - 3 W
CompactFlash	—	100 mW - 300 mW
Gigabit Ethernet (per interface)	—	1.3 W - 1.4 W

5.4 Start-Up Currents of the CP307

The following table indicates the start-up currents of the CP307 with soldered memory during the first 2-3 seconds after the power supply has been switched on. There was no SODIMM memory module mounted on the CP307. The power consumption of the CP307 during operation is indicated in tables 5-4 to 5-7.

Table 5-9: Start-Up Currents of the CP307

POWER		CORE™ Duo 1.2 GHz (ULV)	CORE™ DUO 1.66 GHz (LV)	CORE™ DUO 2.0 GHz (SV)	CORE™2 DUO 1.5 GHz (LV)	CORE™2 DUO 2.16 GHz (SV)
5 V	peak	7.0 A	7.0 A	7.0 A	7.0 A	7.0 A
	average	2.0 A	2.0 A	2.0 A	2.0 A	2.0 A
3.3 V	peak	7.8 A	7.8 A	7.8 A	7.8 A	7.8 A
	average	0.8 A	0.8 A	0.8 A	0.8 A	0.8 A

For further information on the start-up current, please contact Kontron.

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Chapter 6

Thermal Considerations

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6. Thermal Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal requirements when implementing CP307 applications.

6.1 Board Internal Thermal Regulation

The thermal management architecture implemented on the CP307 can be described as being two separate but related functions. The goal of these functions is to protect the processor and reduce processor power consumption. Enabling the thermal control circuit allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

The two thermal protection functions provided by the processor are:

1. Intel® Core™ Duo and Intel® Core™2 Duo Thermal Supervision

   This function controls the processor temperature by SpeedStep® or clock modulation via the internal Digital Thermal Sensor (DTS).

2. Thermtrip:

   In the event of a catastrophic cooling failure resulting in extreme overheating, the processor and/or the 945GM Express GMCH will automatically shut down when the die temperature has reached approximately 125°C. This event is known as “Thermtrip”.

6.1.1 CPU Internal Thermal Supervision

This function can be enabled and disabled in the BIOS, whereby the default value is: enabled. When the internal thermal control circuit has been enabled and a high temperature situation occurs, the internal clocks are controlled by SpeedStep®. If this is not sufficient, the clocks are additionally modulated by alternately turning them off and on with a 50% duty cycle. This results in the reduction of the processor power consumption and the processor performance depending on the active SpeedStep® and the duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. The thermal control circuit is automatically deactivated when the temperature goes below the internal thermal supervision point. The internal temperature sensors are located near to the hottest area of the processor dies. Each processor is individually calibrated during manufacturing to eliminate any potential manufacturing variations.

Note ...

The duty cycle and the internal thermal supervision point is factory configured by Intel and cannot be modified. For all Intel® Core™ Duo and Intel® Core™2 Duo processors the internal thermal supervision point is 100°C.

Note ...

The TH LED on the front panel always shows the status of the internal thermal supervision regardless of whether it is enabled or disabled in the BIOS.

6.1.2 CPU Emergency Thermal Supervision (Thermtrip)

This function cannot be enabled or disabled in the BIOS. It is always enabled to ensure that the processor is protected in any event.

Assertion of Thermtrip indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 125°C. Upon assertion of Thermtrip, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. Once activated, Thermtrip remains latched until the CP307 undergoes a cold restart (all power off and then on again).

Note ...

Upon assertion of Thermtrip, the front panel overtemperature LED flashes at regular intervals.

6.1.3 Thermal Management Recommendations

If the CP307 is operated in a properly configured CompactPCI environment with enough airflow, there is no need to enable the Thermal Management function. However, sometimes the system environment is not optimized for an Intel® Core™ Duo or an Intel® Core™2 Duo processor board and this requires thermal protection to guarantee a stable system. The Thermal Management feature allows system designers to design lower cost thermal solutions without compromising system integrity or reliability.

If the system environment is not optimized for the CP307, the internal Thermal Monitor should be enabled. The internal Thermal Monitor protects the processor and the system against excessive temperatures. In this configuration the clocks will be switched off and on. For example, at a 50% duty cycle, the average power dissipation can drop by up to 50%. In this case, the processor performance also drops by about 50%.

Warning!

For Benchmarks and performance tests the CPU internal Thermal Supervision should be disabled; if enabled, the results will be erroneous due to the thermal power reduction.

6.2 External Thermal Regulation

The thermal management concept of the CP307 also encompasses external thermal regulation. For the Intel® Core™ Duo and Intel® Core™2 Duo processors, a specifically designed heat sink is employed to ensure the best possible basis for operational stability and long-term reliability. Coupled together with system chassis which provide variable configurations for forced airflow, thermal energy dissipation is guaranteed.

6.2.1 Heat Sink

Even though the CP307 is fitted with an optimally designed passive heat sink, it still requires forced airflow which must be provided by the CompactPCI system. For the minimum airflow required, refer to the thermal characteristic graphs in this chapter.

The following heat sink types are used on the CP307:

- Aluminum heat sink for rugged environments used on the CP307 populated with one of the following processors:
  - Core™ Duo 1.2 GHz
  - Core™ Duo 1.66 GHz
  - Core™2 Duo 1.5 GHz
- Copper skived fin heat sink for enhanced thermal conductivity used on the CP307 populated with one of the following processors:
  - Core™ Duo 2.0 GHz
  - Core™2 Duo 2.16 GHz

Figure 6-1: CP307 with Aluminum Heat Sink

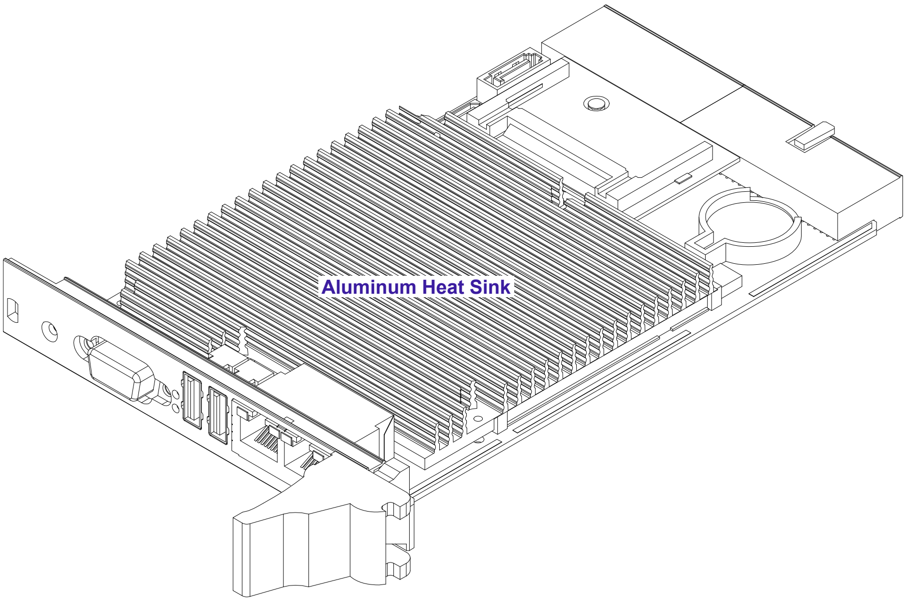
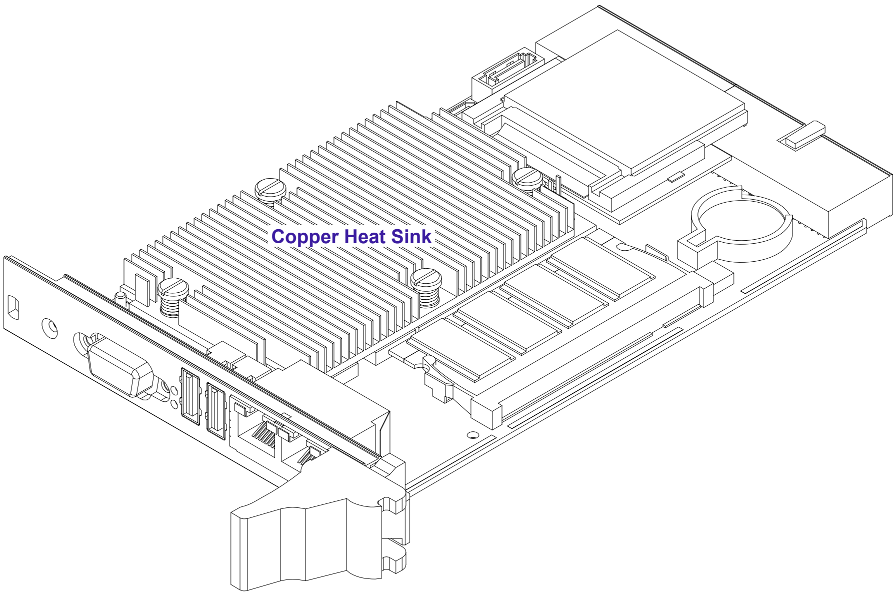


Figure 6-2: CP307 with Copper Heat Sink



6.2.2 Forced Airflow

When developing applications using the CP307, the system integrator must be aware of the overall system thermal requirements. System chassis must be provided which satisfy these requirements. As an aid to the system integrator, characteristics graphs are provided for the CP307.

The values have been measured using typical applications running under Linux/Windows® XP. In worst case situations, the values vary and the temperature range must be reduced. In all situations, the maximum case temperature of the Intel® Core™ Duo and the Intel® Core™2 Duo processors must be kept below the maximum allowable temperature. This temperature value can be measured with the temperature sensor integrated in the CPU. To ensure functionality at the maximum temperature, the BIOS supports a temperature control feature. In instances of overtemperature, the hardware monitor will reduce the power consumption.

The maximum case temperatures for all processor types is as follows:

- Intel® Core™ Duo: all versions: 100°C
- Intel® Core™2 Duo: all versions: 100°C

6.2.3 Thermal Characteristic Graphs

The thermal characteristic graphs shown on the following pages illustrate the maximum ambient air temperature as a function of the volumetric airflow rate for the power consumption indicated. The diagrams are intended to serve as guidance for reconciling board and system with the required computing power considering the thermal aspect. One diagram per CPU version is provided. There are up to two curves representing upper level working points based on different levels of average CPU utilization. When operating below the corresponding curve, the CPU runs steadily without any intervention of thermal supervision. When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop in order to protect the CPU from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

TDP curves

- 100% TDP curve
  This load complies with the maximum thermal design power (TDP) indicated in Chapter 5.2 Power Consumption, Table 5-7. 100% TDP can be achieved through the use of specific tools to heat up the CPU but 100% TDP is unlikely to be reached in real applications.
- 75% TDP curve
  This load represents a "typical" maximum power dissipation reached under OS-controlled applications. Typically, this load corresponds with 75% of the TDP (see Chapter 5.2 Power Consumption, Table 5-6).

How to read the diagram

Select a specific CPU and choose a specific working point. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must not be less than the value specified in the diagram.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth). The volumetric flow rate is specified in m³/h (cubic-meter-per-hour) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 1.7 m³/h; 1 m³/h = 0.59 cfm

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

The airflow is specified in m/s = meter-per-second or in fps = feet-per-second, respectively.

Conversion: 1 fps = 0.3048 m/s; 1 m/s = 3.28 fps

The following figures illustrate the operational limits of the CP307 taking into consideration power consumption vs. ambient air temperature vs. airflow rate. The measurements were made based on a 4HP slot and with both processor cores enabled.

Figure 6-3: Operational Limits for the CP307 with Core™ Duo 1.2 GHz

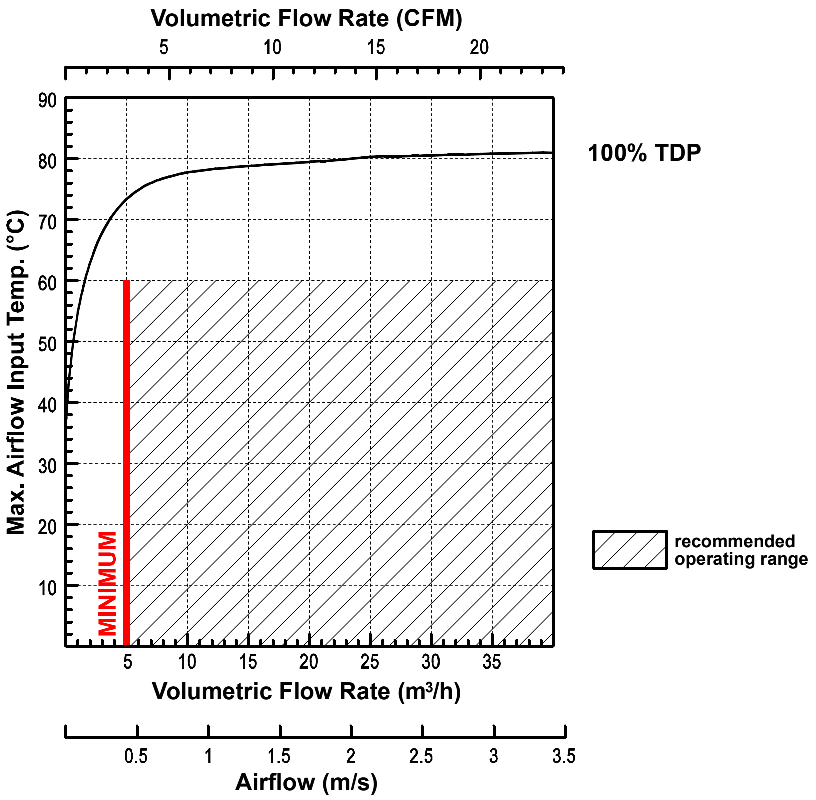


Figure 6-4: Operational Limits for the CP307 with Core™ Duo 1.66 GHz

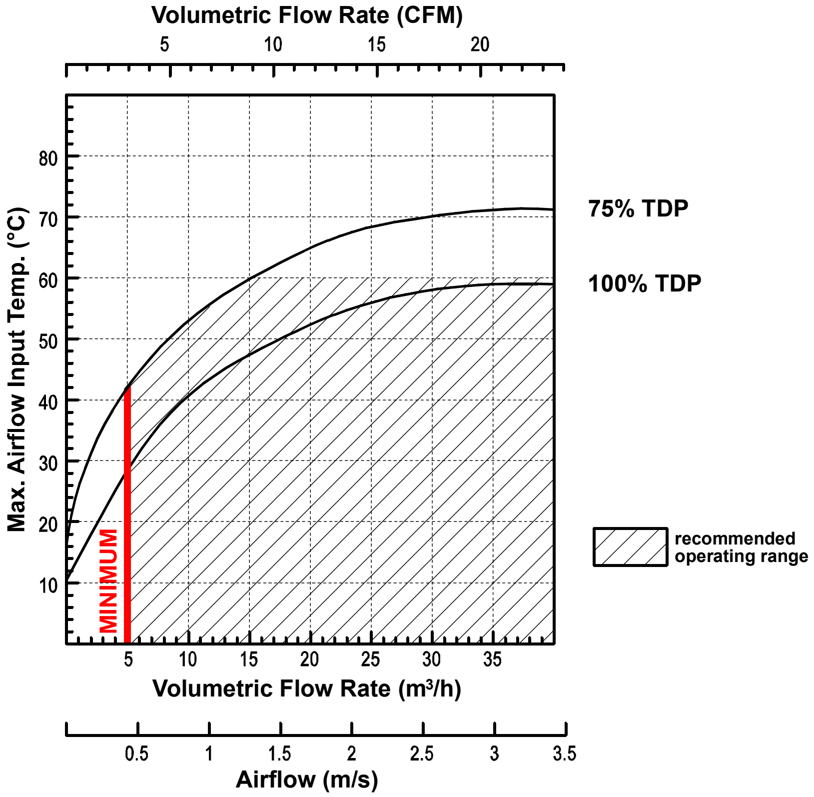


Figure 6-5: Operational Limits for the CP307 with Core™ Duo 2.0 GHz

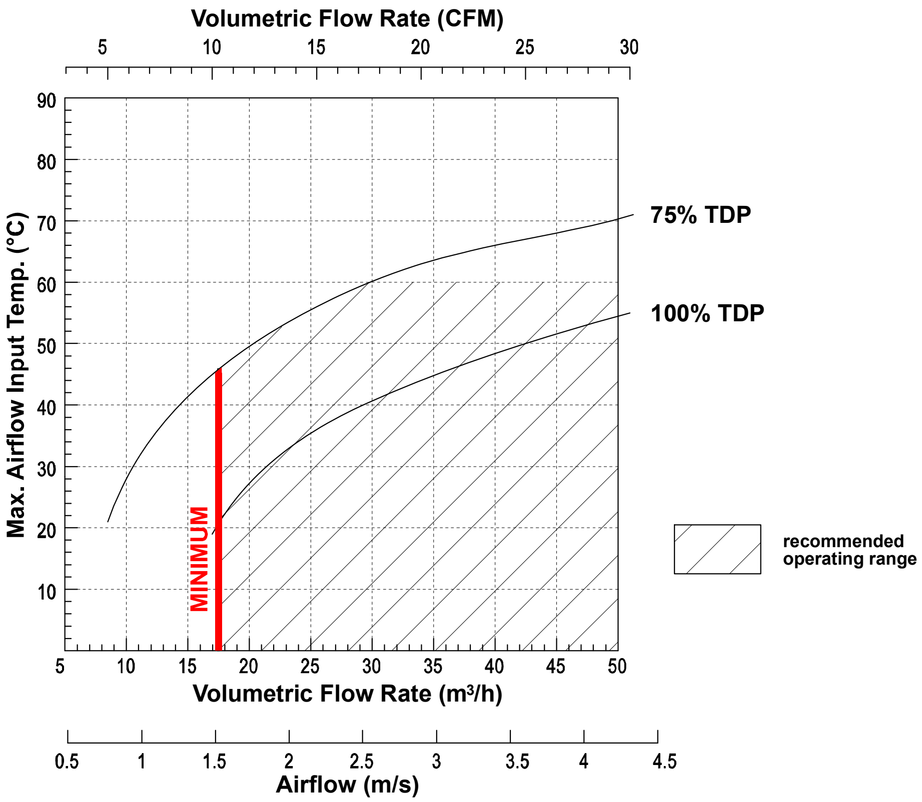


Figure 6-6: Operational Limits for the CP307 with Core™2 Duo 1.5 GHz

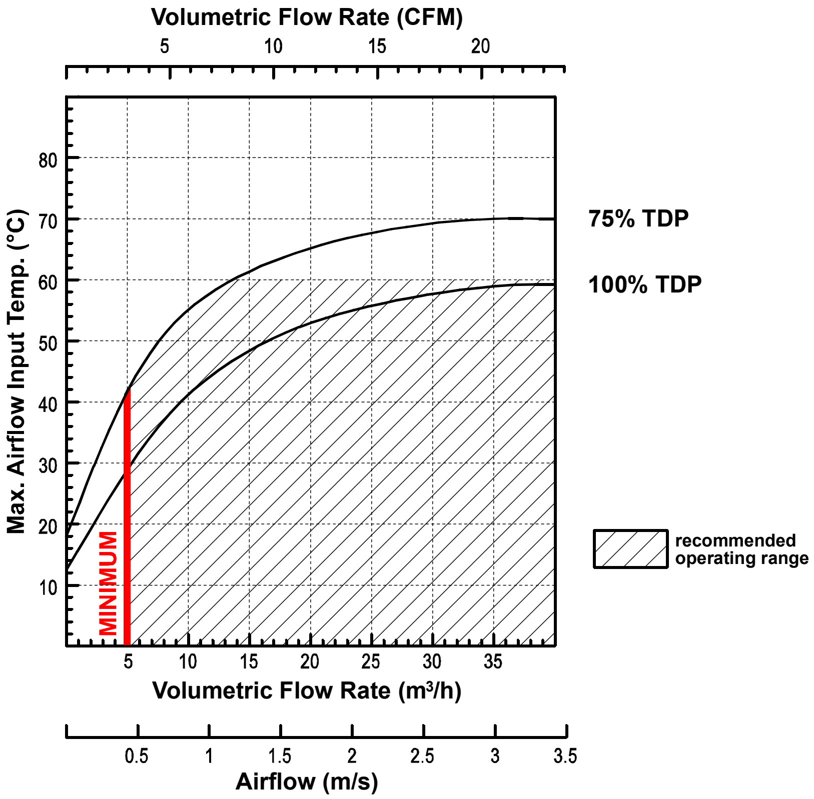
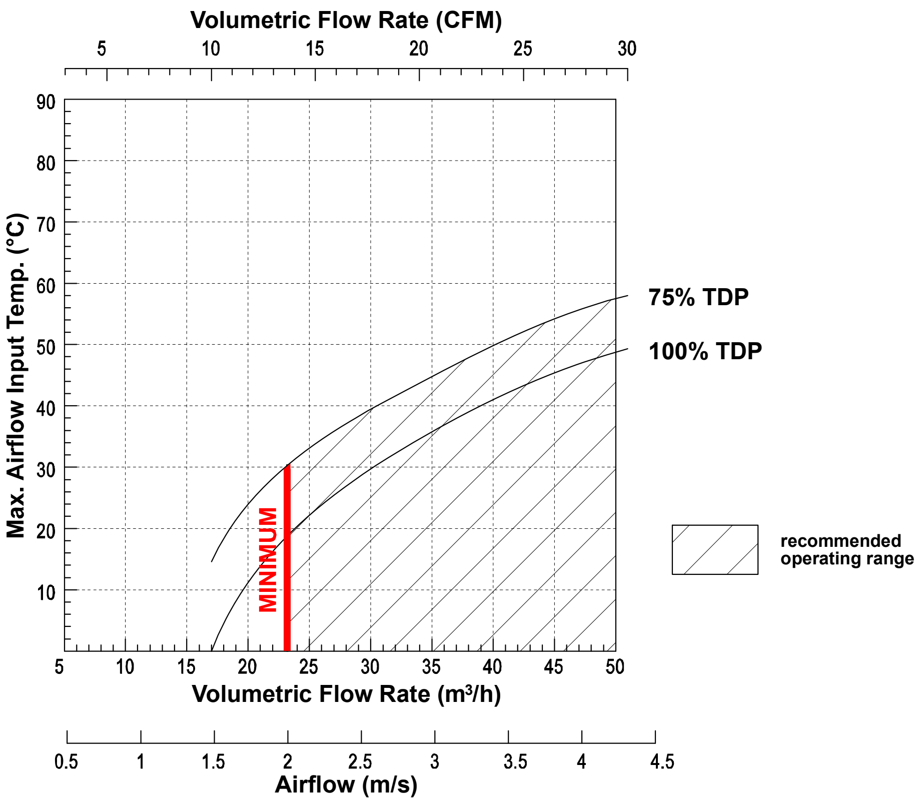


Figure 6-7: Operational Limits for the CP307 with Core™2 Duo 2.16 GHz



An airflow of 1.0 m/s is a typical value for a standard *Kontron* ASM rack (3U CompactPCI rack with a 1U cooling fan tray). Newer ASMs from *Kontron* will have an airspeed of 2.0 m/s or more. For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient operating temperature, the processor junction temperature must never exceed the specified limit for the involved processor type.

6.2.4 Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the CP307 must also be considered. Devices such as hard disks, extension modules, etc. which are directly attached to the CP307 must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions. In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

Warning!

As Kontron assumes no responsibility for any damage to the CP307 or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the CP307 complies with the thermal considerations set forth in this document.

Appendix A

CP307-HDD

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A. CP307-HDD Module

A.1 Overview

The Kontron CP307-HDD module has been designed to include a COM port, a PS/2 keyboard and mouse port, a SATA hard disk interface, and standard IDE interface, two USB 2.0 interfaces, a CompactFlash socket, a DVI-D flat panel interface, a PLCC FWH Flash socket and a battery socket. The CP307-HDD module extends the CP307 version from 4 HP to 8 HP. This additional capability opens up the broadest range of expansion possibilities.

The connectors for the COM port, the PS/2 keyboard and mouse, the USB ports, and the DVI-D port are situated at the front panel, while the SATA hard disk, the CompactFlash socket, and the IDE connectors are onboard connectors. The module connects to the CP307 via I/O extension connectors.

The PLCC FWH Flash socket provides a boot option to the CP307 and can be selected via jumper J1.

The battery socket on the CP307-HDD module has the same function as the battery socket on the CP307.

Note ...

If a CP307-HDD module is used on the CP307, either the CP307 or the CP307-HDD module may be equipped with a battery.

Using one battery on the CP307 and one on the CP307-HDD module simultaneously may result in premature discharge of the batteries.

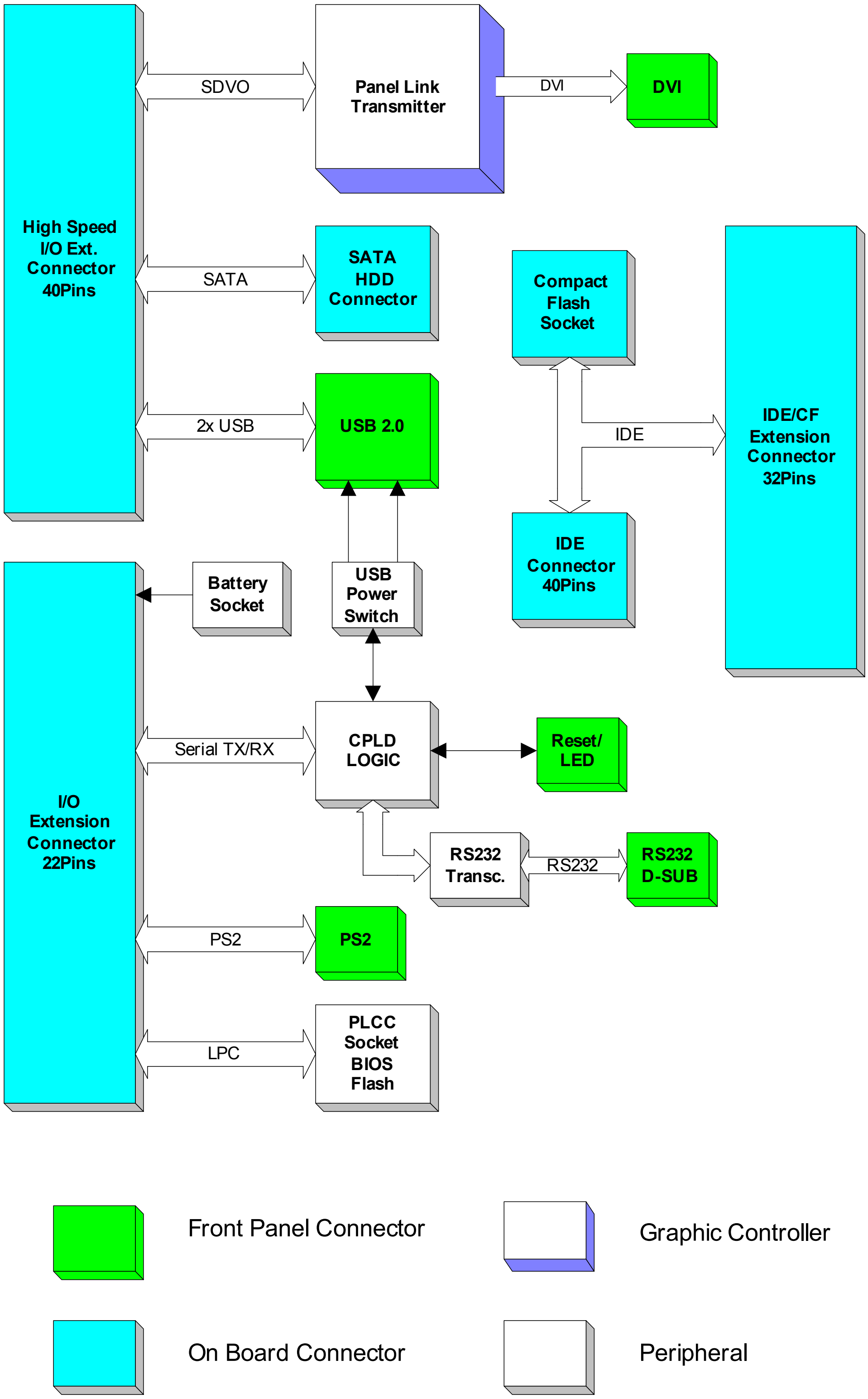
A.2 Technical Specifications

Table A-1: CP307-HDD Module Main Specifications

CP307-HDD		SPECIFICATIONS
External Interfaces	Keyboard and Mouse Interface	PS/2 type, 6-pin, shielded mini-DIN connector for the keyboard and mouse (via Y-cable)
	Serial Port	One 16C550 compatible serial port (COM1), RS-232; 9-pin D-Sub connector
	USB	Two USB 2.0 interfaces
	DVI-D	One DVI-D interface, digital signals only
Internal Interfaces	IDE Interface (PATA)	One IDE interface supporting hard disks or CD/DVD drives on 40-pin, 2.54 mm, onboard connector (only one slave device if CF is installed)
	SATA	SATA interface supporting one 2.5” hard disk drive
	CompactFlash	One CompactFlash, True IDE with DMA (IDE master only)
	PLCC Flash	One PLCC Flash, 32-pin socket providing optional boot
Indicators/ Switches	HDD LED	One LED (green) monitors SATA hard disk activity
	Front Panel Switch	Reset button, guarded
General	Power Consumption	Power consumption without hard disk and without peripheral devices connected: 100 mA at 3.3 V 40 mA at 5.0 V
	Temperature Range	Operational: 0°C to +60°C Standard (depending on processor version and air-flow in the system) -40°C to +85°C E2 (only with Core™ Duo 1.2 GHz; without hard disk and in the appropriate system environment)) Storage: -55°C to +85°C Without hard disk and without battery -40°C to +65°C With hard disk ***Note ...*** When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CP307-HDD module (See "Battery" below). ***Note ...*** When additional components are installed, refer to their operational specifications as this will influence the board’s operational and storage temperature.
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	Dimensions: 100 mm x 150 mm
	Board Weight	CP307 8HP with heat sink: 540 grams (with mounted 2.5” HDD)
	Battery	3.0V lithium battery for RTC with battery socket. Recommended type: CR2025 Temperature ranges: Operational: -20°C to +70°C typical (refer to the battery manufacturer’s specifications for exact range) Storage: -55°C to +70°C typical (no discharge)

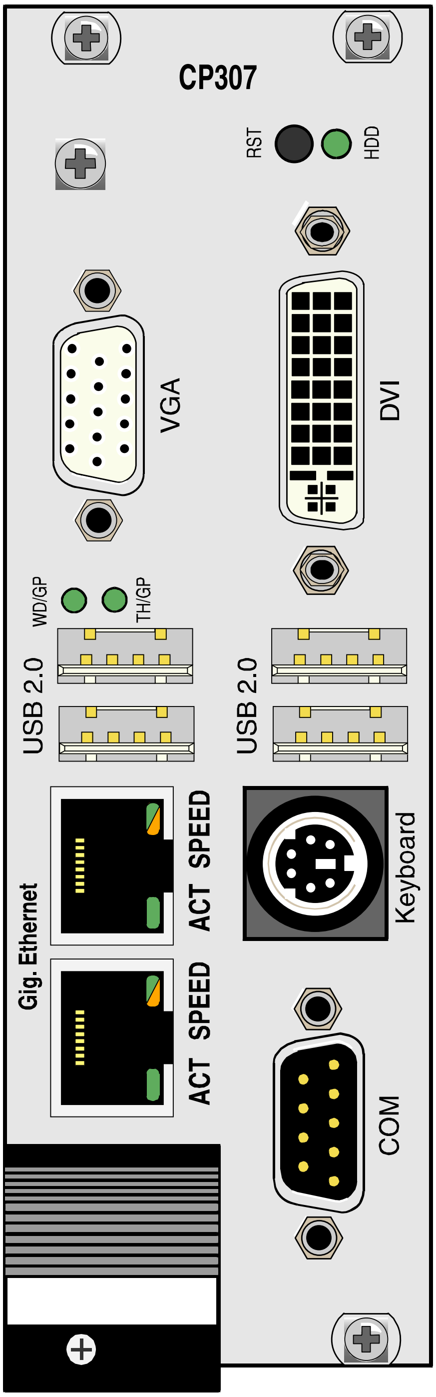
A.3 CP307-HDD Module Functional Block Diagram

Figure A-1: CP307-HDD Module Functional Block Diagram



A.4 Front Panel of 8HP CP307 for CP307-HDD Module

Figure A-2: Front Panel of 8HP CP307 for CP307-HDD Module



LEGEND:

CP307: 8HP version

General Purpose LEDs:

WD/GP (green):	Watchdog or General Purpose; when lit during power-on, it indicates a PCI reset is active.
TH/GP (green):	Overtemperature Status or General Purpose; when lit during power-on, it indicates a power failure.
HDD (green):	Monitors SATA hard disk activity

Note ...

If TH LED and WD LED keep flashing during BIOS initialization, a POST code is indicated.

For further information, please contact Kontron.

Integral Ethernet LEDs:

ACT (green):	Ethernet Link/Activity
SPEED (green/orange):	Ethernet Speed
SPEED ON (orange):	1000 Mbit
SPEED ON (green):	100 Mbit
SPEED OFF:	10 Mbit

A.5 CP307-HDD Module Layout

Figure A-3: CP307-HDD Module Layout (Top View)

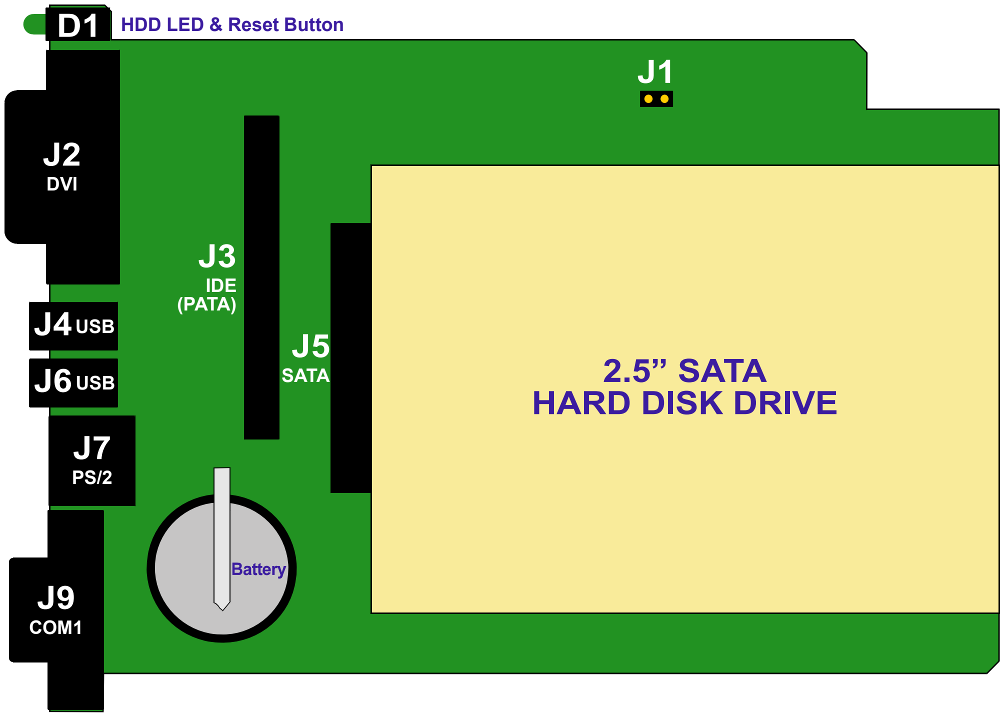
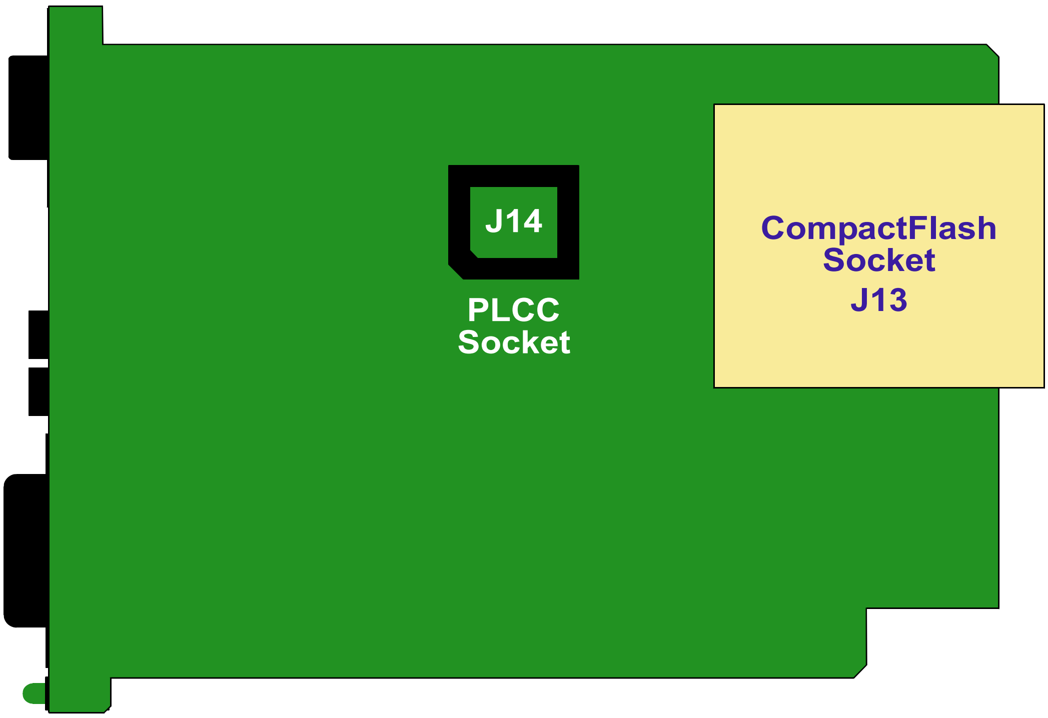


Figure A-4: CP307-HDD Module Layout (Bottom View)



A.6 Module Interfaces (Front Panel and Onboard)

A.6.1 Keyboard/Mouse Interface

The keyboard controller is located on the CP307 and is 8042 software compatible.

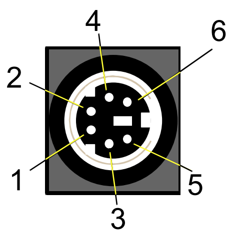
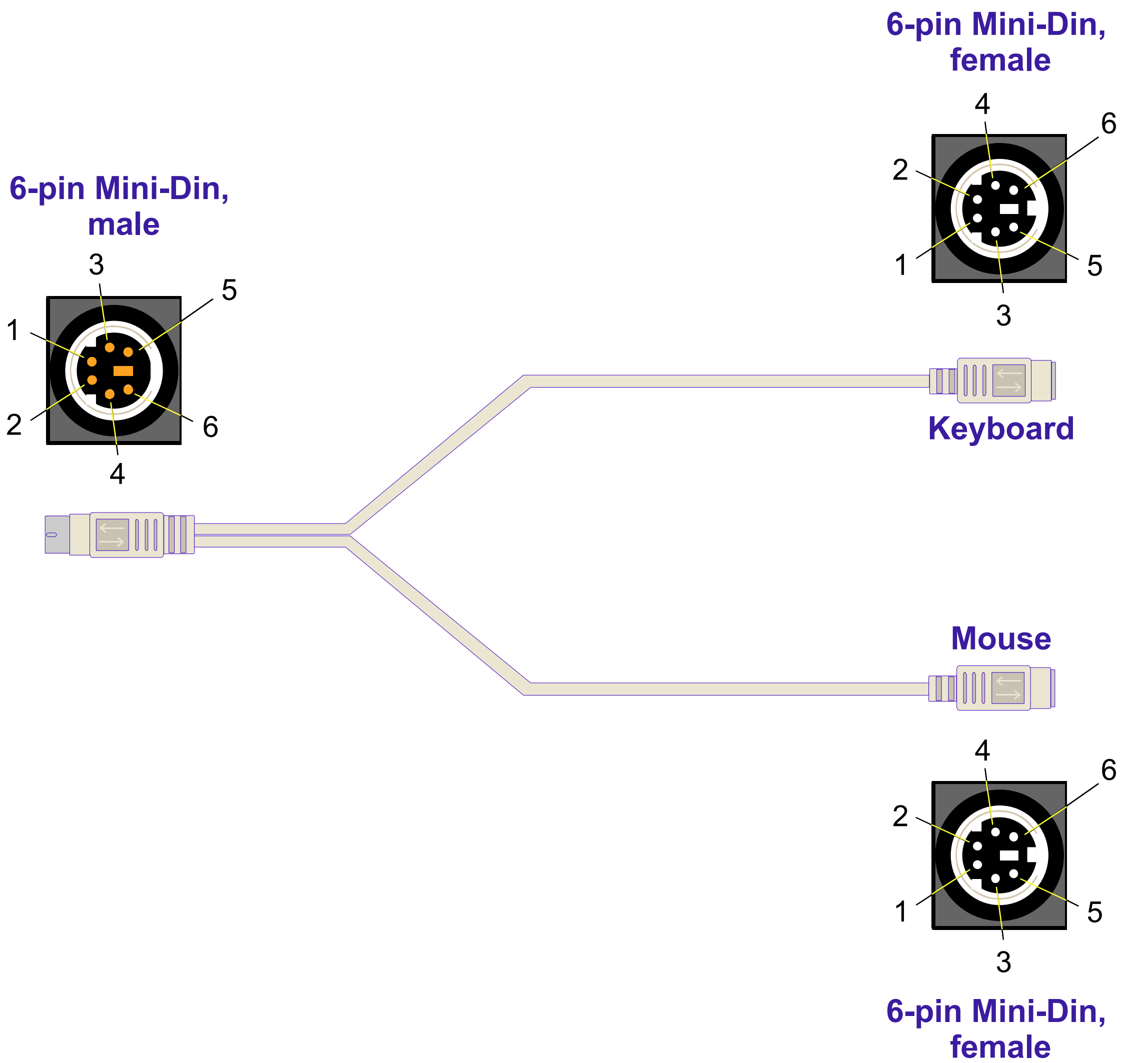


Figure A-5: Keyboard/Mouse Connector

The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded Mini-DIN connector.

A special adapter to connect a mouse device and/or a keyboard to the PS/2 connector ia available from *Kontron.*

Figure A-6: Adapter for Connecting Mouse/Keyboard via PS/2



The CP307 has the AT keyboard connector implemented on a 6-pin Mini-Din connector.

Figure A-7: Keyboard Connector J7 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	KDATA	Keyboard data	I/O
2	MDATA	Mouse data	I/O
3	GND	Ground signal	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	I/O
6	MCLK	Mouse clock	I/O

Note ...

The PS/2 power supply provides short-circuit protection and all the signal lines are EMI-filtered.

A.6.2 Universal Serial Port

One PC-compatible serial RS-232, 9-pin D-Sub port is available which is fully compatible with the 16C550 controller. This port includes a complete set of handshaking and modem control signals. Data transfer rates up to 115.2 kB/s are supported.

The COM1 interface is routed to the serial port connector J9.

Figure A-8: Serial Port Con. J9

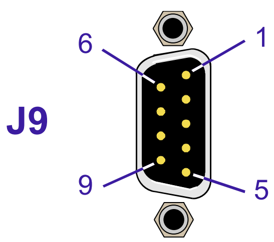


Table A-2: Serial Port Con. J9 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	DCD	Data carrier detect	I
2	RXD	Receive data	I
3	TXD	Transmit data	O
4	DTR	Data terminal ready	O
5	GND	Signal ground	--
6	DSR	Data send request	I
7	RTS	Request to send	O
8	CTS	Clear to send	I
9	RI	Ring indicator	I

A.6.3 USB Interfaces

The CP307-HDD provides two standard USB 2.0 ports on J4 and J6.

The CP307-HDD supports two USB 2.0 ports. The USB 2.0 ports are high-speed, full-speed, and low-speed capable. Hi-speed USB 2.0 allows data transfers of up to 480 Mb/s - 40 times faster than a full-speed USB (USB 1.1).

One USB peripheral may be connected to each port. To connect more USB devices than there are available ports, an external hub is required.

Figure A-9: USB Connectors J4 and J6

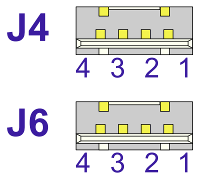


Table A-3: USB Connectors J4 and J6 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND	--

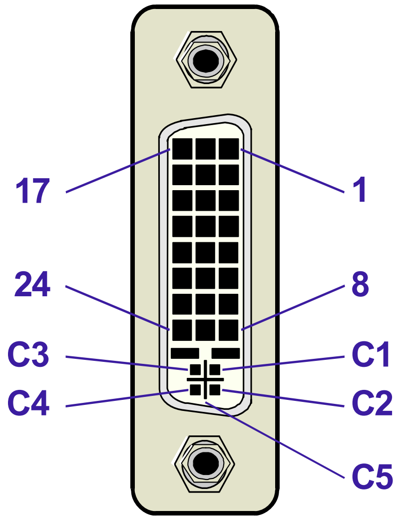
Note ...

The CP307-HDD host interfaces can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

A.6.4 DVI-D Interface

The CP307-HDD provides one standard DVI-D interface, J2, which is a digital signal only interface with device detection.

Figure A-10: DVI-D Connector J2



The following table indicates the pinout of the DVI-D Connector J2.

Table A-4: DVI-D Connector J2 Pinout

PIN	SIGNAL	DESCRIPTION	I/O	PIN	SIGNAL	DESCRIPTION	I/O
1	TMDS Data 2-	TMDS* Link -	O	2	TMDS Data 2+	TMDS* Link +	O
3	GND	Ground	--	4	NC	Not connected	--
5	NC	Not connected	--	6	DDC Clock	I^2C™ Clock	O
7	DDC Data	I^2C™ Data	I/O	8	NC	Not connected	--
9	TMDS Data 1-	TMDS Link -	O	10	TMDS Data 1+	TMDS Link +	O
11	GND	Ground	--	12	NC	Not connected	--
13	NC	Not connected	--	14	VCC	Power +5 V, 1.5A fused	--
15	GND	Ground	--	16	HPDETECT	Hot Plug Detect	I
17	TMDS Data 0-	TMDS Link -	O	18	TMDS Data 0+	TMDS Link +	O
19	GND	Ground	--	20	NC	Not connected	--
21	NC	Not connected	--	22	GND	Ground	--
23	TMDS Clock +	TMDS Link +	O	24	TMDS Clock -	TMDS Link -	O
C1	NC	Not connected	--	C2	NC	Not connected	--
C3	NC	Not connected	--	C4	NC	Not connected	--
C5	GND	Ground	--				

* TMDS = Transition Minimized Differential Signaling

A.6.5 IDE Interface (PATA)

The IDE interface on the CP307-HDD module is comprised of the connector J3 and the CompactFlash socket. The J3 connector is used to connect external devices to the CP307-HDD module.

J3 is a standard 40-pin 2.54mm pinrow connector. Up to two devices (which must be master/slave pairs) may be attached to the CP307-HDD board.

Note ...

Only one external IDE slave device may be connected to the IDE connector J3 if a CompactFlash card is installed. This is due to the fact that an installed CompactFlash card is always configured as IDE master.

Note ...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. Please contact Kontron for further information.

A wide range of IDE devices may be connected to the CP307-HDD module at J3 using a ribbon cable. The following table describes the pinout of connector J3.

Table A-5: Pinout of IDE Connector J3

I/O	DESCRIPTION	SIGNAL	PIN	PIN	SIGNAL	DESCRIPTION	I/O
O	Reset HD	IDERESET	1	2	GND	Ground signal	--
I/O	HD data 7	HD7	3	4	HD8	HD data 8	I/O
I/O	HD data 6	HD6	5	6	HD9	HD data 9	I/O
I/O	HD data 5	HD5	7	8	HD10	HD data 10	I/O
I/O	HD data 4	HD4	9	10	HD11	HD data 11	I/O
I/O	HD data 3	HD3	11	12	HD12	HD data 12	I/O
I/O	HD data 2	HD2	13	14	HD13	HD data 13	I/O
I/O	HD data 1	HD1	15	16	HD14	HD data 14	I/O
I/O	HD data 0	HD0	17	18	HD15	HD data 15	I/O
--	Ground signal	GND	19	20	NC	KEY	--
I	DMA request	IDEDRQ	21	22	GND	Ground signal	--
O	I/O write	IOW	23	24	GND	Ground signal	--
O	I/O read	IOR	25	26	GND	Ground signal	--
I	I/O channel ready	IOCHRDY	27	28	CSEL	Cable select	I/O
O	DMA Ack	IDEDACKA	29	30	GND	Ground signal	--
I	Interrupt request	IDEIRQ	31	32	IOCS16	Obsolete	I/O
O	Address 1	A1	33	34	PDIAG#/ CBLID#*	Detect ATA100	I
O	Address 0	A0	35	36	A2	Address 2	O
O	HD select 0	HCS0	37	38	HCS1	HD select 1	O
I	LED driving	LED	39	40	GND	Ground signal	--

* Signal terminated with 10 kΩ pull-down resistor

A.6.6 CompactFlash Socket

To enable flexible flash extension, a CompactFlash (CF) type II socket, J13, is available on the CP307-HDD.

CompactFlash is a very small removable mass storage device. It provides true IDE functionality compatible with the 16-bit ATA/ATAPI-4 interface.

The CompactFlash socket is connected to the IDE port of the ICH7-R and is set to master configuration.

The CP307 supports DMA and both CF type I and CF type II.

Note ...

An installed CompactFlash card is always configured as IDE master. For this reason, only one additional external IDE slave device may be connected to the CP307-HDD if a CompactFlash card is installed.

The following table provides the pinout for the CompactFlash connector J13.

Table A-6: CompactFlash Connector J13 Pinout

I/O	FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION	I/O
--	Ground Signal	GND	1	2	D03	Data 3	I/O
I/O	Data 4	D04	3	4	D05	Data 5	I/O
I/O	Data 6	D06	5	6	D07	Data 7	I/O
O	Chip Select 0	IDE_CS0	7	8	GND (A10)	--	--
--	--	GND (ATASEL)	9	10	GND (A09)	--	--
--	--	GND (A08)	11	12	GND (A07)	--	--
--	Power 5 V	VCC	13	14	GND (A06)	--	--
--	--	GND (A05)	15	16	GND (A04)	--	--
--	--	GND (A03)	17	18	A02	Address 2	O
O	Address 1	A01	19	20	A00	Address 0	O
I/O	Data 0	D00	21	22	D01	Data 1	I/O
I/O	Data 2	D02	23	24	IOCS16	Obsolete	I/O
--	--	NC (CD2)	25	26	NC (CD1)	--	--
I/O	Data 11	D11	27	28	D12	Data 12	I/O
I/O	Data 13	D13	29	30	D14	Data 14	I/O
I/O	Data 15	D15	31	32	IDE_CS1	Chip Select 1	O
--	--	NC (VS1)	33	34	IORD	I/O Read	O
O	I/O Write	IOWR	35	36	VCC (WE)	Power 5 V	--
I	Interrupt Request	INTRQ	37	38	VCC	Power 5 V	--
O	Master/Slave	CSEL (GND/pull-up)	39	40	NC (VS2)	--	--
O	Reset	Reset	41	42	IORDY	I/O Ready	I
I	DMA Request	DMARQ	43	44	DMACK	DMA Acknowl-edge	O
I/O	Drive Active Slave Present	DASP	45	46	PDIAG#/ CBLID#*	--	--
I/O	Data 08	D08	47	48	D09	Data 09	I/O
I/O	Data 10	D10	49	50	GND	Ground Signal	--

* Signal terminated with 10 kΩ pull-down resistor

Note ...

The CompactFlash socket on the CP307-HDD supports all available Compact-Flash cards type I and type II with 5 V power supply.

A.6.7 SATA Interface (SATA2)

The SATA connector, J5, on the CP307-HDD module is provided for connecting a 2.5” SATA HDD to the CP307-HDD module. The SATA connector is divided into two segments, a signal segment and a power segment.

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Figure A-11: SATA Connector J5

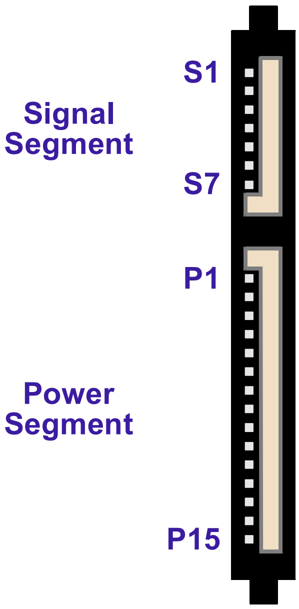

Table A-7: SATA Connector J5 Pinout

PIN	SIGNAL	FUNCTION	I/O
Signal Segment Key			
S1	GND	Ground signal	--
S2	SATA_TX2+	Differential Transmit+	O
S3	SATA_TX2-	Differential Transmit-	O
S4	GND	Ground signal	--
S5	SATA_RX2-	Differential Receive-	I
S6	SATA_RX2+	Differential Receive+	I
S7	GND	Ground signal	--
Signal Segment “L”			
Central Connector Polarizer			
Power Segment “L”			
P1	3.3V	3.3V power	--
P2	3.3V	3.3V power	--
P3	3.3V	3.3V power	--
P4	GND	Ground signal	--
P5	GND	Ground signal	--
P6	GND	Ground signal	--
P7	5V	5V power	--
P8	5V	5V power	--
P9	5V	5V power	--
P10	GND	Ground signal	--
P11	RES	Reserved	--
P12	GND	Ground signal	--
P13	NC (12V)	Not connected	--
P14	NC (12V)	Not connected	--
P15	NC (12V)	Not connected	--
Power Segment Key			

A.6.8 PLCC Socket

A 32-pin PLCC socket, J14, is available for installing a FWH flash on the CP307-HDD module. This flash can be used for booting the CP307 in case of a crash of the onboard firmware hub flash. The jumper J1 must be set prior to applying power to the system in order to boot the CP307 from the FWH flash on the CP307-HDD module.

A.6.9 Battery

The CP307-HDD may be equipped with a 3.0 V “coin cell” lithium battery for the RTC on the CP307.

Note ...

If a CP307-HDD module is used on the CP307, either the CP307 or the CP307-HDD module may be equipped with a battery.

Using one battery on the CP307 and one on the CP307-HDD module simultaneously may result in premature discharge of the batteries.

To replace the battery, proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery type CR2025.

Note ...

The user must be aware that the battery’s operational temperature range is less than the CP307-HDD’s storage temperature range.

For exact range information, refer to the battery manufacturer’s specifications.

Note ...

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer’s instructions.

The typical life expectancy of a 170 mAh battery (CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.

To ensure that the lifetime of the battery has not been exceeded, it is recommended to exchange the battery after 4 - 5 years.

Appendix B

CP-RIO3-04 Rear I/O

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B. CP-RIO3-04 Rear I/O Module

B.1 Overview

The CP307 provides optional Rear I/O connectivity for peripherals, a feature which may be particularly useful in specialized CompactPCI systems. Some standard PC interfaces are implemented and assigned to the front panel and to the Rear I/O connector J2 on the CP307.

When the CP-RIO3-04 Rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus, the CP-RIO3-04 Rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system Rear I/O feature a special backplane is necessary. The CPU board with Rear I/O is compatible with all standard CompactPCI passive backplanes with Rear I/O support on the system slot.

The CP-RIO3-04 Rear I/O Module provides the following interfaces.

- CompactPCI Rear I/O
- Two USB 2.0 ports
- Two Gigabit Ethernet ports without LED signals
- Two COM ports
- VGA analog port
- Two SATA ports
- One fan monitor input
- One fan control output (PWM)
- Power supply management

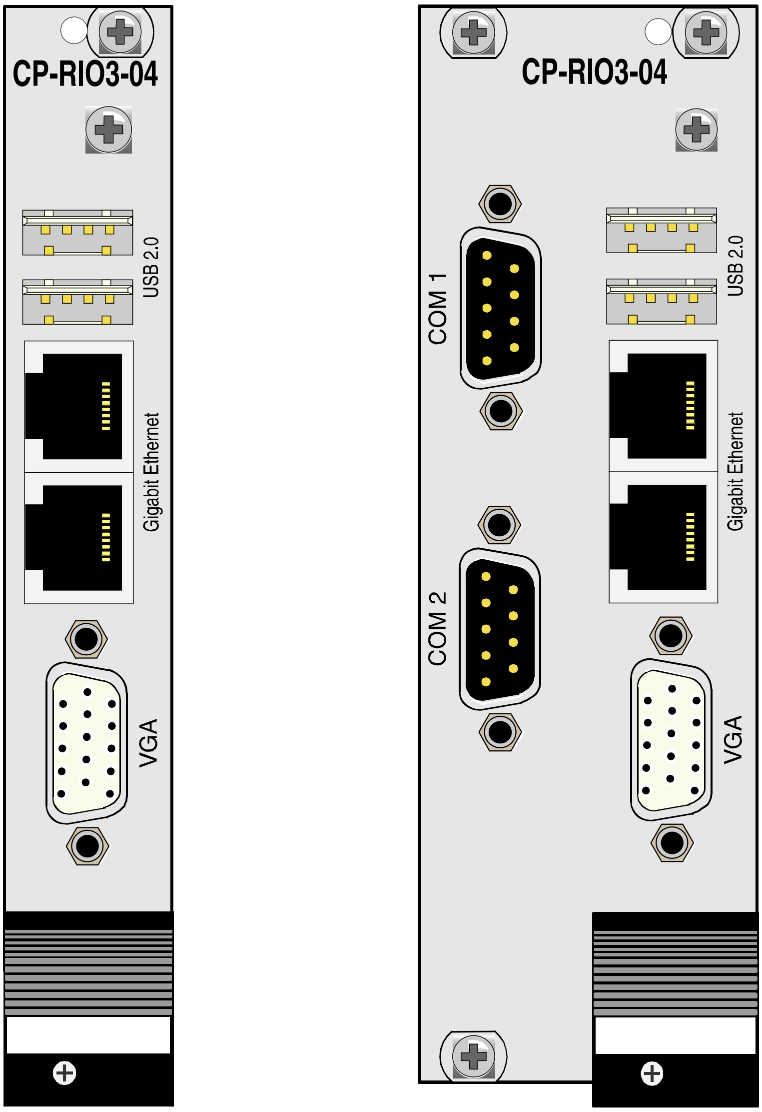
B.2 Technical Specifications

Table B-1: CP-RIO3-04 Rear I/O Module Main Specifications

CP-RIO3-04 Rear I/O		SPECIFICATIONS
External Interfaces	USB	Two USB 2.0 interfaces; two 4-pin connectors
	VGA	One VGA interface; 15-pin D-Sub connector
	Ethernet	Two Gigabit Ethernet interfaces implemented as dual RJ-45 connector without LEDs
	COM	Two serial ports (COM1 and COM2), RS-232; 9-pin D-Sub connectors (8HP only), full modem support
Internal Interfaces	SATA	Two SATA interfaces; SATA1 and SATA2
	Peripheral Control	One 10-pin, 2.54 mm onboard connector • One fan monitor input • One fan control output (PWM) • Power supply management
	Compact PCI	CompactPCI connector for connecting Rear I/O to the backplane
	COM	Two COM ports implemented as two 10-pin, 2.54 mm onboard connectors (4HP only) full modem support
General	Temperature Range	Operational: 0°C to +60°C Storage: -55°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 80 mm
	Board Weight	4 HP: 120 grams 8HP: 150 grams

B.3 Front Panels

Figure B-1: CP-RIO3-04 Front Panels, 4HP and 8HP Versions



4 HP

8 HP

B.4 Module Layout: 4HP and 8HP Versions

Figure B-2: CP-RIO3-04 Module Layout, 4HP Version

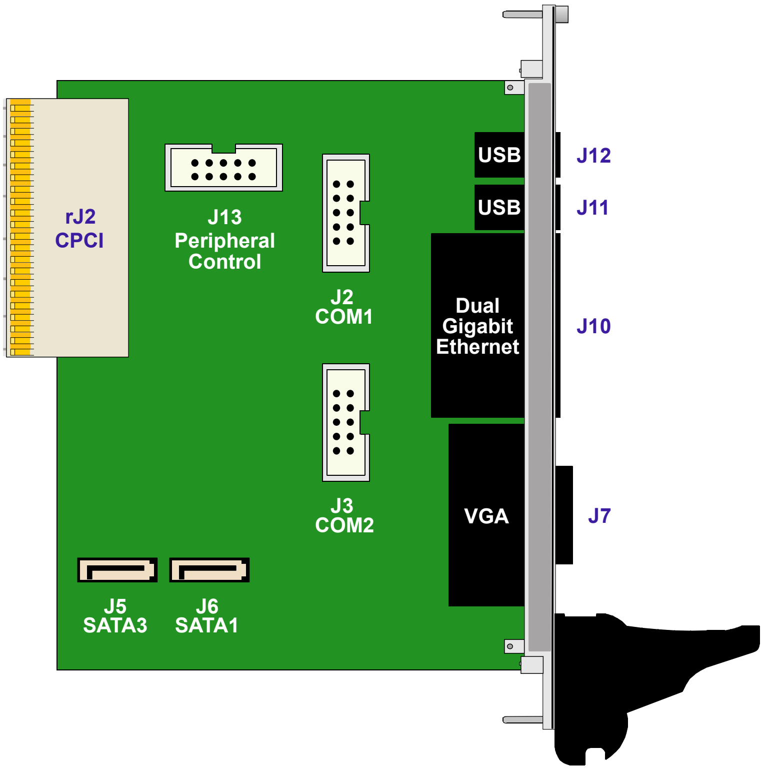
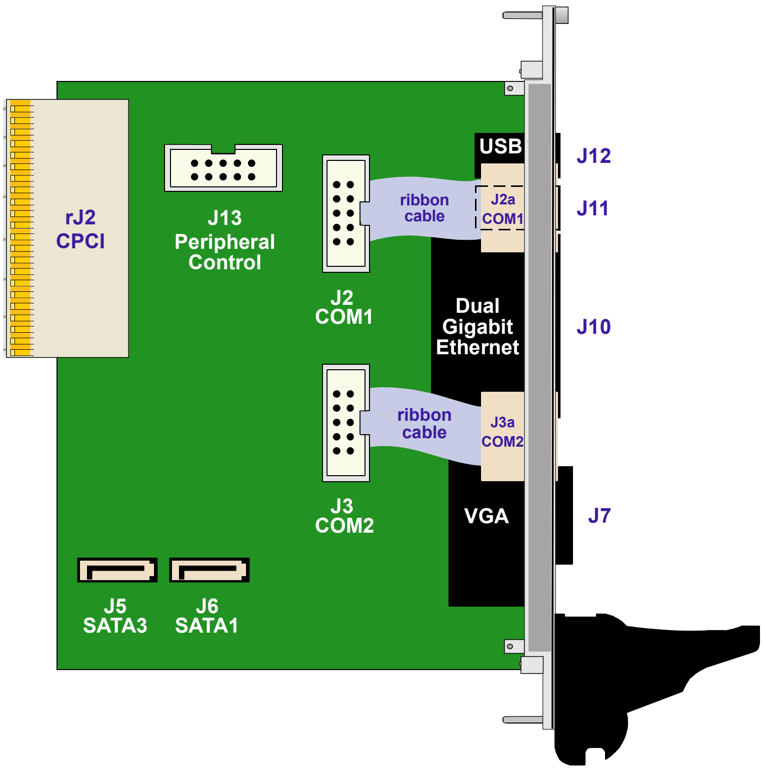


Figure B-3: CP-RIO3-04 Module Layout, 8HP Version



B.5 Module Interfaces

B.5.1 USB Interfaces

There are two identical USB interfaces on the CP-RIO3-04 Rear I/O module, each with a maximum transfer rate of 480 Mb/s provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more USB devices than there are available ports, an external hub is required.

Figure B-4: USB Connectors J11/J12

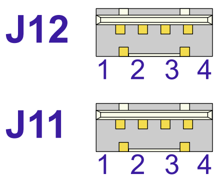


Table B-2: USB Con. J11 and J12 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	VCC	VCC signal	O
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND signal	--

Note ...

The USB host interfaces on the CP-RIO3-04 Rear I/O module can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

Note ...

The Rear I/O interface supports the USB 1.1 and USB 2.0 standards. For USB 2.0 it is strongly recommended to use a cable length not exceeding 3 meters.

B.5.2 VGA Interface

The 15-pin female connector J7 is used to connect a VGA monitor to the CP-RIO3-04 Rear I/O module.

Figure B-5: D-Sub VGA Con. J7

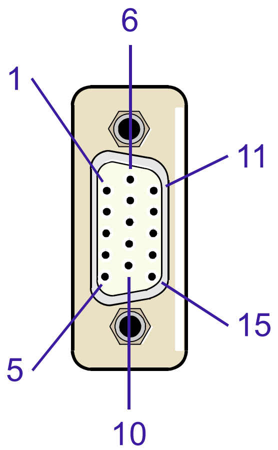


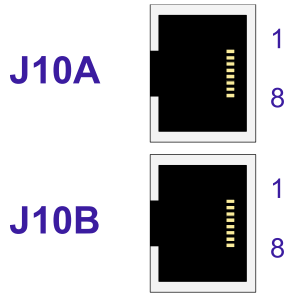
Table B-3: D-Sub VGA Connector J7 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	Red	Red video signal output	O
2	Green	Green video signal output	O
3	Blue	Blue video signal output	O
13	Hsync	Horizontal sync.	TTL Out
14	Vsync	Vertical sync.	TTL Out
12	Sdata	I^2C data	I/O
15	Sclk	I^2C clock	O
9	VCC	Power +5V, 140 mA fuse protection	O
5,6,7,8, 10	GND	Ground signal	--
4,11	NC	--	--

B.5.3 Gigabit Ethernet Interface

The Ethernet connectors are realized as RJ-45 connectors. The interface provides automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Figure B-6: Dual Gigabit Ethernet Connector J10A/B



RJ-45 Connector J10A/B Pinouts

The J10A/B connector supplies the 10Base-T, 100Base-TX and 1000Base-T interfaces to the Ethernet controller.

Table B-4: Pinouts of J10A/B Based on the Implementation

MDI / STANDARD ETHERNET CABLE						PIN	MDIX / CROSSED ETHERNET CABLE					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	RX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

Note ...

The Ethernet transmission can operate effectively with structured cable that meets CAT5 cable or higher specifications.

B.5.4 COM Interface

The CP-RIO3-04 Rear I/O module provides two identical COM ports for connecting RS-232 devices to the CP-RIO3-04 Rear I/O module.

On the 8HP version, the onboard 10-pin COM connectors J2 and J3 are routed to the 9-pin D-Sub COM connectors J2a and J3a located on the front panel.

On the 4HP version, the COM signals are available only on the onboard 10-pin COM connectors J2 and J3 connectors.

The following figure and table provide pinout information for the 9-pin D-Sub COM connectors J2a and J3a located on the front panel.

Figure B-7: COM Connectors J2a (COM1) and J3a (COM2)

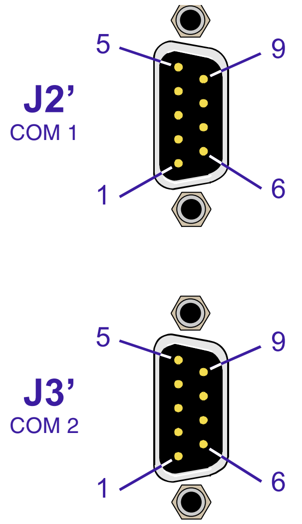


Table B-5: COM Connectors J2a (COM1) and J3a (COM2) Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	DCD	Data carrier detect	I
2	RXD	Receive data	I
3	TXD	Transmit data	O
4	DTR	Data terminal ready	O
5	GND	Signal ground	--
6	DSR	Data send request	I
7	RTS	Request to send	O
8	CTS	Clear to send	I
9	RI	Ring indicator	I

The following figure and table provide pinout information for the onboard COM connectors J2 and J3.

Figure B-8: Serial Port Connectors J2 (COM1) and J3 (COM2)

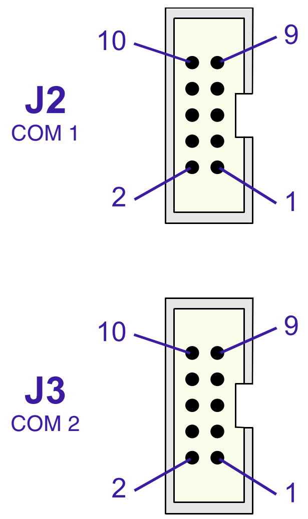


Table B-6: Serial Port Connectors J2 (COM1) and J3 (COM2) Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	DCD	Data carrier detect	I
2	DSR	Data send request	I
3	RXD	Receive data	I
4	RTS	Request to send	O
5	TXD	Transmit data	O
6	CTS	Clear to send	I
7	DTR	Data terminal ready	O
8	RI	Ring indicator	I
9	GND	Signal ground	--
10	NC	Not connected	--

B.5.5 Peripheral Control Interface

A fan for system cooling and a power supply with power management can be connected via the peripheral control connector J13.

The following figure and table provide pinout information for the power connector J13.

Figure B-9: Peripheral Connector J13

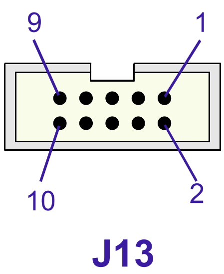


Table B-7: Peripheral Connector J13 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	GND	Signal ground	--
2	PWR_5VSTDBY	+5V standby power (optional)	I
3	FAN_SENSE	Fan speed monitor	I
4	VCC5V	Power +5V	O
5	PWM_OUT	Fan speed control via pulse with modulation signal	O
6	VCC3V3	Power +3.3V	O
7	PWR_SLPS3#	Power supply sleep mode	O
8	GND	Signal ground	--
9	PWR_BTN#	Wake-up / sleep input	I
10	GND	Signal ground	--

Note ...

Pin 5 is an open drain output and has no pull-up resistor on the CP-RIO3-04 Rear I/O module. Therefore, for fan control operations, an external pull-up resistor is required.

B.5.6 Serial ATA Interfaces SATA1 and SATA3

The onboard Serial ATA connectors J5 and J6 allow the connection of standard HDDs and other Serial ATA devices to the CP-RIO3-04 Rear I/O module.

The following figure and table provide pinout information for the SATA connectors J5 and J6.

Figure B-10:SATA Con. J5 and J6

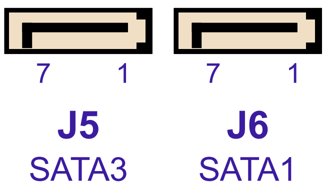


Table B-8: SATA Connectors J5 and J6 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	GND	Ground signal	--
2	SATA_TX+	Differential Transmit +	O
3	SATA_TX-	Differential Transmit -	O
4	GND	Ground signal	--
5	SATA_RX-	Differential Receive -	I
6	SATA_RX+	Differential Receive +	I
7	GND	Ground signal	--

Note ...

When using a Serial ATA cable, it is recommended to use a special right-angled Serial ATA cable due to possible space limitations within the system. For further information, please contact Kontron.

B.5.7 Rear I/O interface on Compact PCI Connector rJ2

The CP-RIO3-04 Rear I/O module conducts a wide range of I/O signals through the Rear I/O connector rJ2.

Warning!

To support the Rear I/O feature a special backplane is necessary. Do not plug a Rear I/O configured board in a non-system slot Rear I/O backplane. Failure to comply with the above may result in damage to your board.

Figure B-11: Rear I/O CompactPCI Connector rJ2

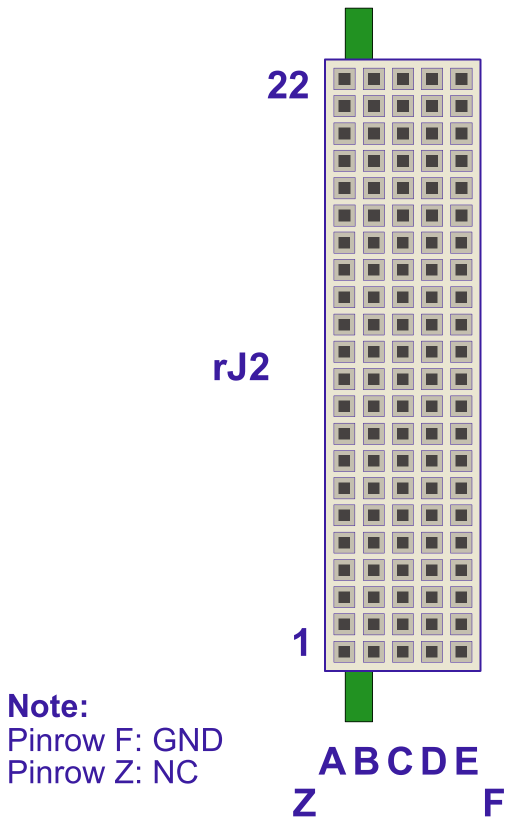


Table B-9: Rear I/O CompactPCI Connector rJ2 Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	NC	NC	NC	NC	NC	NC	GND
21	NC	NC	GND	USB1P / bi	USB3P / bi	USB1_5V / in	GND
20	NC	NC	GND	USB1N / bi	USB3N / bi	USB3_5V / in	GND
19	NC	GND	GND	PWR_BTN# / out	PWR_SLPS3# / in	RIO_3.3V / in	GND
18	NC	1RXD / out	1DCD / out	1DTR / in	2CTS / out	1CTS / out	GND
17	NC	1TXD / in	2RXD / out	NC	NC	NC	GND
16	NC	1DSR / out	1RTS / in	NC	RSV	1RI / out	GND
15	NC	PWR_5VSTDBY / out	FAN_SENSE / out	NC	NC	NC	GND
14	NC	IPA_DA+ / bi	IPA_DA- / bi	2RTS /in	IPA_DC+ / bi	IPA_DC- / bi	GND
13	NC	IPA_DB+ / bi	IPA_DB- / bi	2RI / out	IPA_DD+ / bi	IPA_DD- / bi	GND
12	NC	IPB_DA+ / bi	IPB_DA- / bi	RIO_2V5 / in	IPB_DC+ / bi	IPB_DC- / bi	GND
11	NC	IPB_DB+ / bi	IPB_DB- / bi	2DCD / out	IPB_DD+ / bi	IPB_DD- / bi	GND
10	NC	GND	2TXD / in	VGA_RED / in	2DTR / in	GND	GND
9	NC	SATA3TXP / in	GND	VGA_HSYNC / in	GND	SATA1TXP / in	GND
8	NC	SATA3TXN / in	GND	VGA_BLUE / in	GND	SATA1TXN / in	GND
7	NC	GND	2DSR / out	VGA_I2C_DAT / bi	PWM_OUT / in OD	GND	GND
6	NC	SATA3RXP / out	GND	VGA_GREEN / in	GND	SATA1RXP / out	GND
5	NC	SATA3RXN / out	GND	VGA_VSYNC / in	GND	SATA1RXN / out	GND
4	NC	NC	RIO_5V / in	VGA_I2C_CLK / in	GPIO_CFG0 / out	GND	GND
3	NC	NC	GND	NC	NC	NC	GND
2	NC	NC	NC	NC	NC	NC	GND
1	NC	NC	NC	NC	NC	NC	GND

Warning!

The RIO_XXX signals are power supply **INPUTS** to supply the Rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a Rear I/O module.

Failure to comply with the above will result in damage to your board.

Legend for Table B-4:

SATAx	Serial ATA port
IPx	Gigabit Ethernet port
USBx	USB interface and power
VGAx	VGA signals
COM1x	COM1 port
GPIOx	COM2 port or GPIO
PWRx	Power Management signals
5V/3.3V	Power
GPIO_CFG0	GPIO configuration (GPIO or COM2)

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