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BD429/BD429A/BD429B ARINC 429/RS-422 Line Driver Integrated Circuit

Features:

- ARINC 429 Line Driver for HI speed (100 kHz) and LOW speed (12.5 kHz) data rates
- Pin for Pin replacement part for industry standard ARINC 429 Line Drivers
- Available in a 16 Pin SOIC (WB), 16 Pin CERDIP, 16 Pin Plastic Dip, 16 Lead Ceramic SOP, and 28L PLCC
- Low EMI RS-422 line driver mode for data rates up to 100 kHz
- Adjustable slew rates via two external capacitors
- Inputs are TTL and CMOS compatible
- Low quiescent power of 125mW (typical)
- Programmable output differential range via V_{REF} pin
- Outputs are fused for failsafe overvoltage protection
- Drives full ARINC load of 400Ω and 30,000pF
- Extended (-55°C/+85°C) and Military (-55°C/+125°C) temperature ranges
- 100% Final Testing

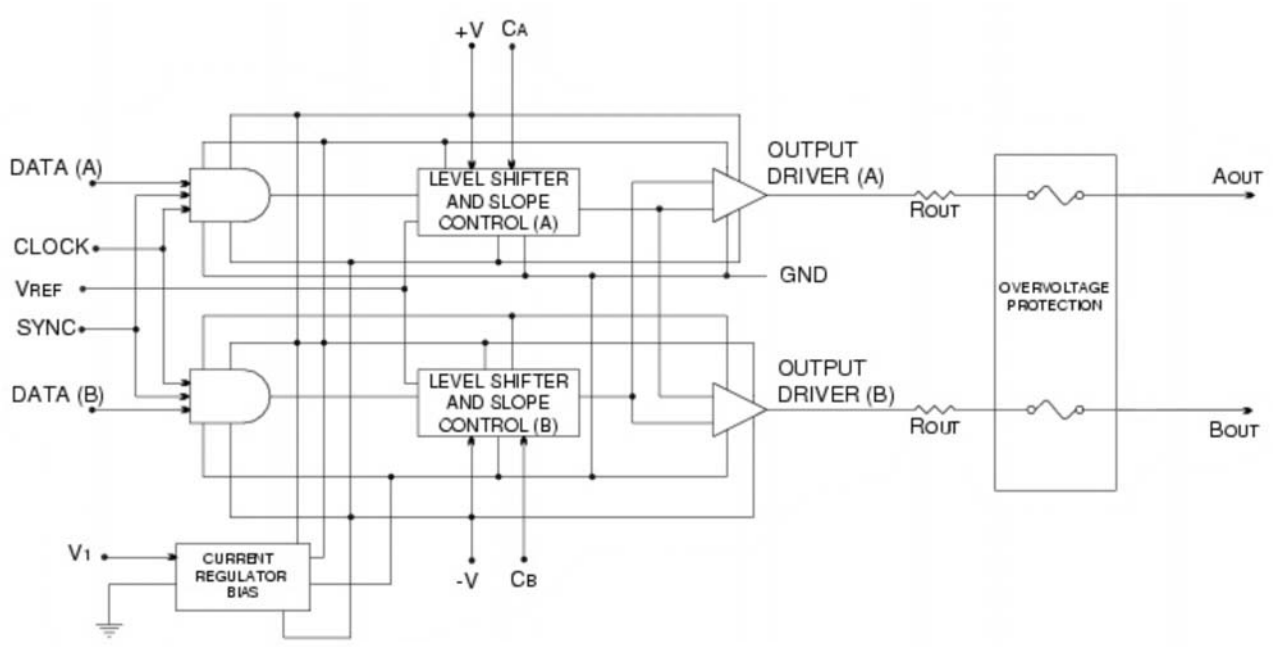


Figure 1: BD429 Block Diagram

DS-MP-00429 Rev. F
03/11/2004

General Description:

The BD429 ARINC Line Driver Circuit is a bipolar monolithic IC designed to meet the requirements of several general aviation serial data bus standards. These include the differential bipolar RZ types such as ARINC 429, ARINC 571, and ARINC 575, as well as the differential NRZ types such as the RS-422 standard.

Functional Description:

Modes: The BD429 operates in either a 429 mode or a 422 mode as controlled by the 429/422´ pin.

429 Mode: In 429 mode, the serial data is presented on the DATA(A) and DATA(B) inputs in the dual rail format defined in the *MARK 33 Digital Information Transfer System – ARINC Specification 429-10*. The driver is enabled by the SYNC and CLOCK inputs. The output voltage level is programmed by the V_{REF} input and is normally tied to +5VDC along with V_1 to produce output levels of +5 volts, 0 volts, and –5 volts on each output for ±10 volts differential outputs. *See figure 4.

422 Mode: In 422 mode, the serial data is presented on DATA(A) input. The driver is enabled by the SYNC and CLOCK inputs. The outputs swings between 0 volts and +5 volts if V_{REF} is at +5VDC. *See figure 5.

Output Resistance: The driver output resistance is 75Ω ±20% at room temperature; 37.5Ω on each output. The outputs are also fused for failsafe protection against shorts to aircraft power. The output slew rate is controlled by external timing capacitors on C_A and C_B. Typical values are 75pF for 100 KHz data and 500pF for 12.5 KHz data.

Table 1: Truth Table

	429/422' NOTE 1	SYNC NOTE 2	CLOCK NOTE 2	DATA(A) NOTE 2	DATA(B) NOTE 2	A_{OUT}	B_{OUT}	COMMENTS
429 MODE	H	L	X	X	X	0	0	NULL
	H	X	L	X	X	0	0	NULL
	H	H	H	L	L	0	0	NULL
	H	H	H	H	H	0	0	NULL
	H	H	H	H	L	$+V_{REF}$	$-V_{REF}$	LOGIC 1
	H	H	H	L	H	$-V_{REF}$	$+V_{REF}$	LOGIC 0
422 MODE	L	L	X	X	X	$+V_{REF}$	0	NULL
	L	X	L	X	X	$+V_{REF}$	0	NULL
	L	H	H	L	X	0	$+V_{REF}$	LOGIC 0
	L	H	H	H	X	$+V_{REF}$	0	LOGIC 1

NOTES:

1. The 429/422' pin is internally pulled up to V_1 through a 10kΩ resistor. So, if no external connection is made to this pin, it will force the chip into the 429 mode.
2. X = Don't care.

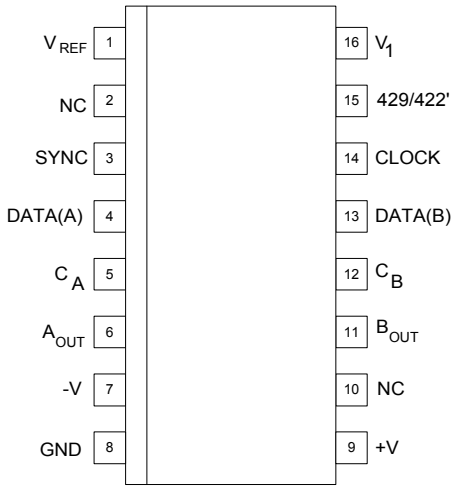


Figure 2: DIP, SOIC, & CSOP Pinout

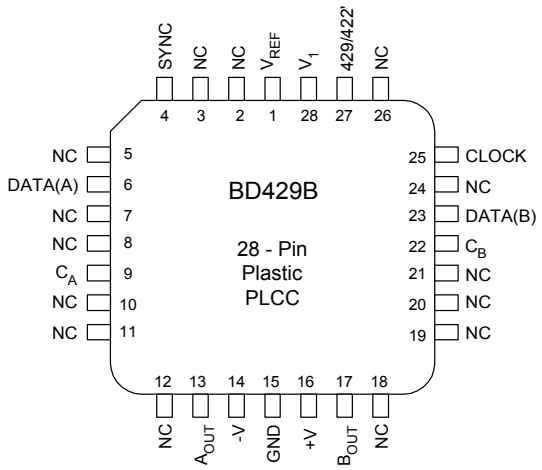


Figure 3: PLCC Pinout

Table 2: Pin Descriptions

Pin Name	Description
V_{REF}	Analog Input. The voltage on V_{REF} sets the output voltage levels on A_{OUT} and B_{OUT}. The output logic levels swing between $+V_{REF}$, 0 volts, and $-V_{REF}$ volts.
NC	No Connect
SYNC	Logic input. Logic 0 forces outputs to NULL state. Logic 1 enables data transmission.
DATA(A) DATA(B)	Logic inputs. These signals contain the Serial Data to be transmitted on the ARINC 429 data bus. Refer to Figures 4 and 5.
C_A C_B	Analog Nodes. External timing capacitors are tied from these points to ground to establish the output signal slew rate. Typical $C_A = C_B = 75pF$ for 100 kHz data and $C_A = C_B = 500pF$ for 12.5 kHz data. *
A_{OUT} B_{OUT}	Outputs. These are the line driver outputs which are connected to the aircraft serial data bus.
-V	Negative Supply Input. –15VDC nominal.
GND	Ground.
+V	Positive Supply Input. +15VDC nominal.
CLOCK	Logic input. Logic 0 forces outputs to NULL state. Logic 1 enables data transmission.
429/422'	Logic Input. Mode control for ARINC 429 and RS-422 modes. An internal 10KΩ pull up resistor keeps the chip in ARINC 429 mode when there is no external connection. This creates a default logic 1, enabling the ARINC 429 mode. A forced logic 0 enables the RS-422 mode.
V_1	Logic Supply Input. +5VDC nominal.

*C_A and C_B pin voltages swing between ±5 volts. Any electronic switching of the capacitor on the pins must not inhibit the full voltage swings.

Table 3: Absolute Maximum Ratings			
PARAMETER	SYMBOL	RATING	UNITS
Voltage between pins +V and –V		40	V
V_1 Maximum Voltage	V_1	7	V
V_{REF} Maximum Voltage	V_{REF}	6	V
DATA(A) Max Input Voltage DATA(B) Max Input Voltage	$V_{DATA(A)}$ $V_{DATA(B)}$	(GND-0.3V) to (V_1 + 0.3V)	V
Lead Soldering Temperature (10 sec duration)	T_{SLD}	280	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Max Junction Temperature Ceramic Package & Plastic Package short term operation	$T_{J\ MAX1}$	+175	°C
Max Junction Temperature Plastic Package Limit (prolonged operation)	$T_{J\ MAX2}$	+145	°C
Output Short Circuit Duration	See Note 1		
Output Over-Voltage Protection	See Note 2		
Power Dissipation	See Table 5 below		

Notes.
1. One output at a time can be shorted to ground indefinitely.
2. Both outputs are fused at between 0.5 Amp DC and 1.0 Amp DC to prevent an over-voltage fault from coupling onto the system power bus.

Table 4: Operating Range					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Positive Supply Voltage	+V	+11.4		16.5	VDC
Negative Supply Voltage	-V	-11.4		-16.5	VDC
V_1	V_1	+4.75	+5	+5.25	VDC
V_{REF} (For ARINC 429)	V_{REF}	+4.75	+5	+5.25	VDC
V_{REF} (For other applications)	V_{REF}	+3		+6	VDC
Operating Temperature (Plastic Package)	T_A	-55		+85	°C
Operating Temperature (Ceramic Package)	T_A	-55		+125	°C

Thermal Management

Device power dissipation varies greatly as a function of data rate, load capacitance, data duty cycle, and supply voltage. Proper thermal management is important in designs operating at the HI speed data rate (100KBS) with high capacitive loads and high data duty cycles.

Power dissipation may be estimated from Table 5 “Power Dissipation Table”. Device power dissipation (Pd) is indicated for 100% data duty cycle with no word gap null times and should be adjusted for the appropriate data duty cycle (DC). Pd(application) = DC * [Pd(table) - 145mW] + 145mW, where DC is the application data duty cycle, Pd(table) is the Pd from the table for the indicated data rate and bus load, and 145mW is the quiescent power. The application’s data duty cycle (DC) for 100KBS operation is calculated as:

DC = (total bits transmitted in 10 sec period / 1,000,000) =
(32 x total ARINC words transmitted in 10 sec period / 1,000,000).

Heat transfer from the IC package should be maximized. Use maximum trace width on all power and signal connections at the IC. Place vias on the signal/power traces close to the IC to maximize heat flow to the internal power planes. If possible, design a solid heat spreader land under and beyond the IC to maximize heat flow from the device.

Table 5: Power Dissipation Table						
100% Duty Cycle, Full Load = 400Ω/30,000pF Half Load = 4,000Ω/10,000pF						
DATA RATE	LOAD	+V @ 15V	-V @ -15V	$V_1 + V_{REF}$ @5V	Pd 429 POWER	LOAD POWER
0 to 100kbps	NONE	2.0mA	-5.0mA	4mA	125mW	0.0mW
12.5kbps	FULL	16.0mA	19.0mA	4mA	485mW	60.0mW
100kbps	FULL	48.0mA	51.0mA	4mA	1194mW	325.0mW
12.5kbps	HALF	6.0mA	8.0mW	4mA	196mW	30.0mW
100kbps	HALF	22.0mA	25.0mA	4mA	561mW	162.5mW

Table 6: DC Electrical Characteristics						
Conditions: Temperature: -55°C to +125°C Ceramic, -55°C to +85°C Plastic, +V = +11.4VDC to +16.5VDC, –V = -11.4VDC to –16.5VDC; $V_1 = V_{REF}$ = +5VDC ±5%, 429/422' = Open Circuit (unless otherwise noted.)						
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
IQ+V	Quiescent +V supply current	-	2	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
IQ-V	Quiescent -V supply current	-	5	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
IQV_1	Quiescent V_1 supply current	-	4	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
IQV_{REF}	Quiescent V_{REF} supply current	-	10	-	µA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
V_{IH}	Logic 1 Input V	2.0	-	-	V	No Load.
V_{IL}	Logic 0 Input V	-	-	0.6	V	No Load.
I_{IH}	Logic 1 Input I	-	-	10	µA	No Load.
I_{IL}	Logic 0 Input I	-	-	-20	µA	No Load. (429/422´ Pin I_{IL} = -2mA max)
I_{OHSC}	Output Short Circuit Current (Output High)	-80	-	-	mA	Short to Ground
I_{OLSC}	Output Short Circuit Current (Output Low)	80	-	-	mA	Short to Ground
V_{OH}	Output Voltage HIGH. (+1)	V_{REF} - 250mV	V_{REF}	V_{REF} + 250mV	V	No Load. 429 Mode.
V_{NULL}	Output Voltage NULL. (0)	-250	-	+250	mV	No Load. 429 Mode.
V_{OL}	Output Voltage LOW. (-1)	$-V_{REF}$ – 250mV	$-V_{REF}$	$-V_{REF}$ + 250mV	V	No Load. 429 Mode.
I_{CT} + -	Timing Capacitor Charge Current C_A (+1) C_B (-1) C_A (-1) C_B (+1)	-	 +200 –200	-	 µA µA	No Load. 429 Mode. SYNC = CLOCK = HIGH C_A and C_B held at zero volts.
ISC (+V)	+V Short Circuit Supply Current	-	-	+150	mA	Output short to ground
ISC (-V)	-V Short Circuit Supply Current	-	-	-150	mA	Output short to ground
R_{OUT}	Resistance on each output	-	37.5	-	Ω	Room Temp Only
C_{IN}	Input Capacitor	-	-	15	pF	-

AC ELECTRICAL CHARACTERISTICS

Figures 4 and 5 show the output waveforms for the ARINC 429 and RS-422 modes of operation.

The output slew rates are controlled by timing capacitors C_A and C_B. They are charged by ±200μA (nom.) Slew rate (SR) measured as V/μsec, is calculated by:

SR = 200/C
where C is in pF.

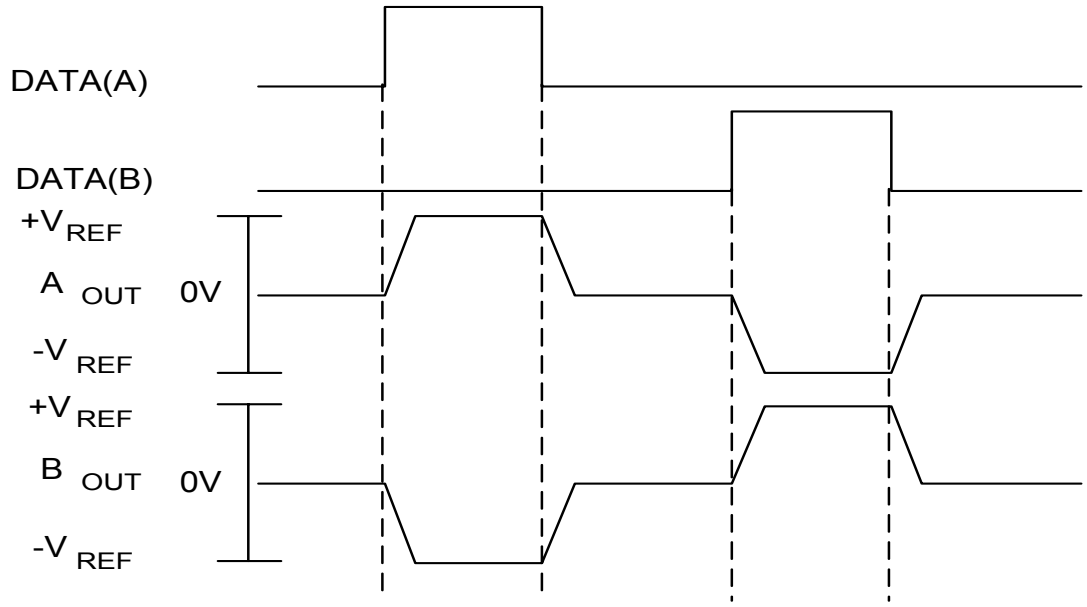


Figure 4: ARINC 429 Waveforms

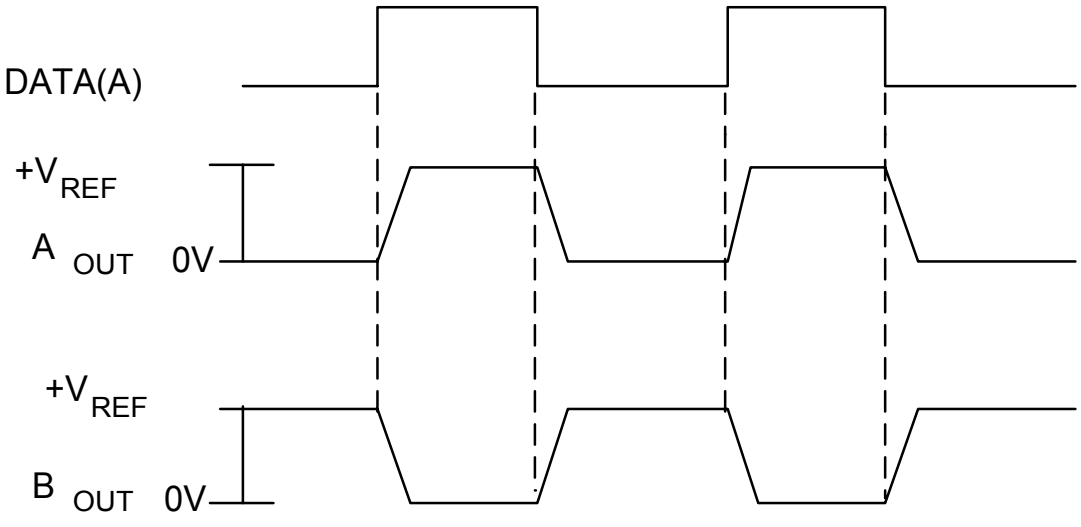
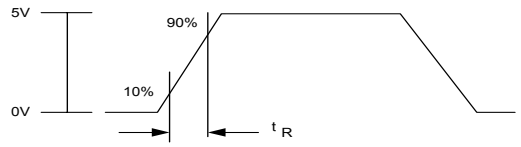
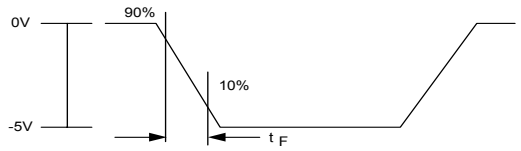


Figure 5: RS-422 Waveforms

Table 7: AC Electrical Characteristics					
Parameter	Symbol	MIN	MAX	UNITS	NOTES
Output Rise Time A_{OUT} or B_{OUT} $C_A = C_B = 75pF$ $C_A = C_B = 500pF$	 t_R t_R	 1.0 5.0	 2.0 15.0	 µsec µsec	
Output Fall Time A_{OUT} or B_{OUT} $C_A = C_B = 75pF$ $C_A = C_B = 500pF$	 t_F t_F	 1.0 5.0	 2.0 15.0	 µsec µsec	
Input to Output Propagation Delay	t_{PNH} t_{PNL}	-	3.0	µsec	See Figure 6 below
A_{OUT} / B_{OUT} Skew Spec.	-	-	500	nsec	

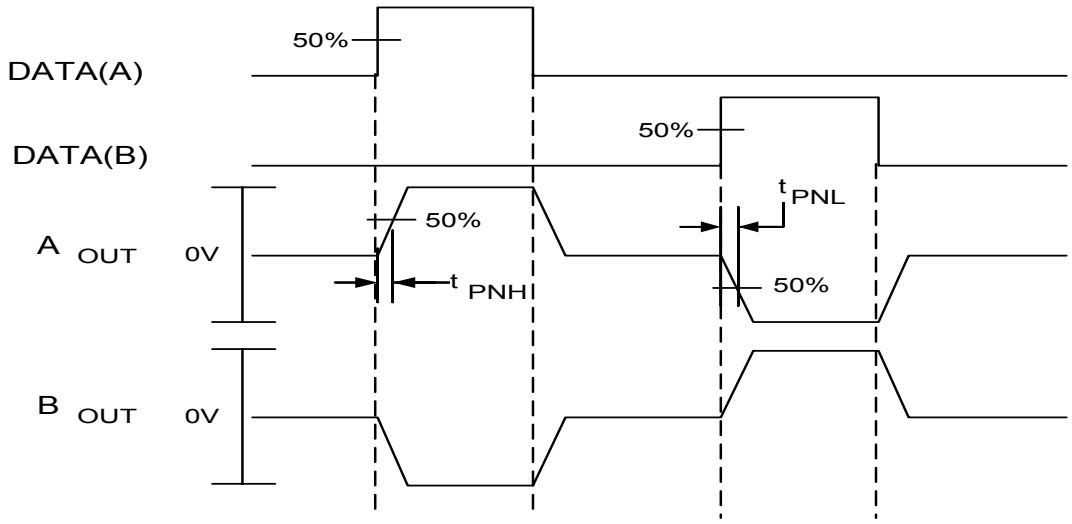


Figure 6: Propagation Delay

Table 8: BD429 Ordering Information				
DEI PART NUMBER	**MARKING (1)**	**PACKAGE**	**TEMP RANGE**	**PROCESSING**
BD429	BD429	16 CERDIP	-55 / +125 °C	CERAMIC BURN IN
BD429A	BD429A	16 SOIC WB	-55 / +85 °C	PLASTIC STANDARD
BD429A1	BD429A1	16 SOIC WB	-55 / +85 °C	PLASTIC BURN IN
BD429B	BD429B	28 PLCC	-55 / +85 °C	PLASTIC STANDARD
DEI0429-NES (2)	DEI0429-NES	16 PDIP	-55 / +85 °C	PLASTIC STANDARD
DEI0429-WMS	DEI0429-WMS	16 CSOP	-55 / +125 °C	CERAMIC STANDARD
DEI0429-WMB	DEI0429-WMB	16 CSOP	-55 / +125 °C	CERAMIC BURN IN

Notes:
1. All packages marked with Lot Code and Date Code.
2. Suffix legend: -XYZ: X = package code, Y = temperature range code, Z = process flow code.

Table 9: BD429 Screening Process				
	PLASTIC STANDARD	**PLASTIC BURN IN**	**CERAMIC STANDARD**	**CERAMIC BURN IN**
THERMAL CYCLE MIL-STD-883B M1010.4 Condition B	NO	NO	10 Cycles	10 Cycles
GROSS & FINE LEAK	NO	NO	YES	YES
BURN IN MIL-STD-883B M1015 Condition A	NO	160 hrs @ +125 °C	NO	96 hrs @ +125 °C
ELECTRICAL TEST:				
ROOM TEMPERATURE	100%	100%	100%	100%
HIGH TEMPERATURE	100% @ +125 °C	100% @ +125 °C	100% @ +125 °C	100% @ +125 °C
LOW TEMPERATURE	0.65% AQL@-55°C	0.65% AQL@-55°C	0.65% AQL@-55°C	0.65% AQL@-55°C

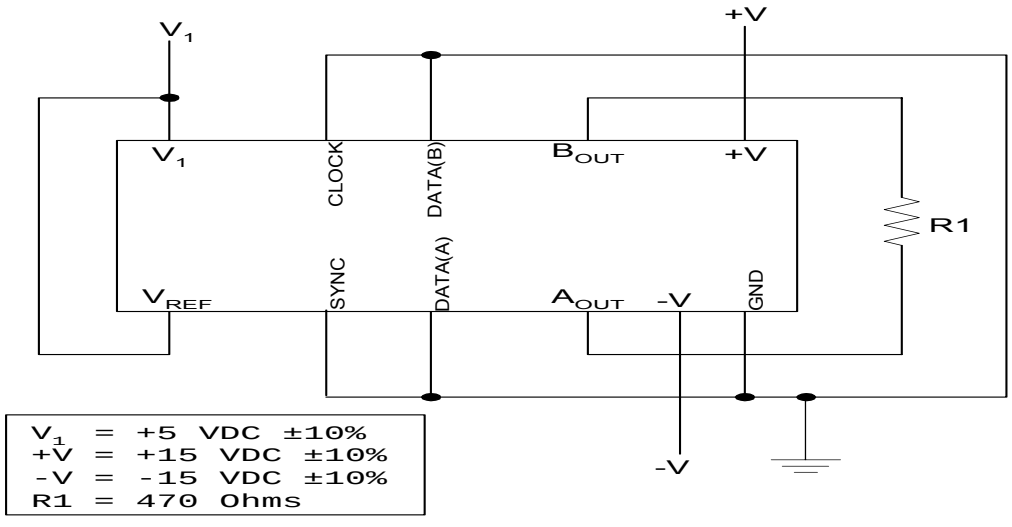


Figure 7: Burn-in Schematic

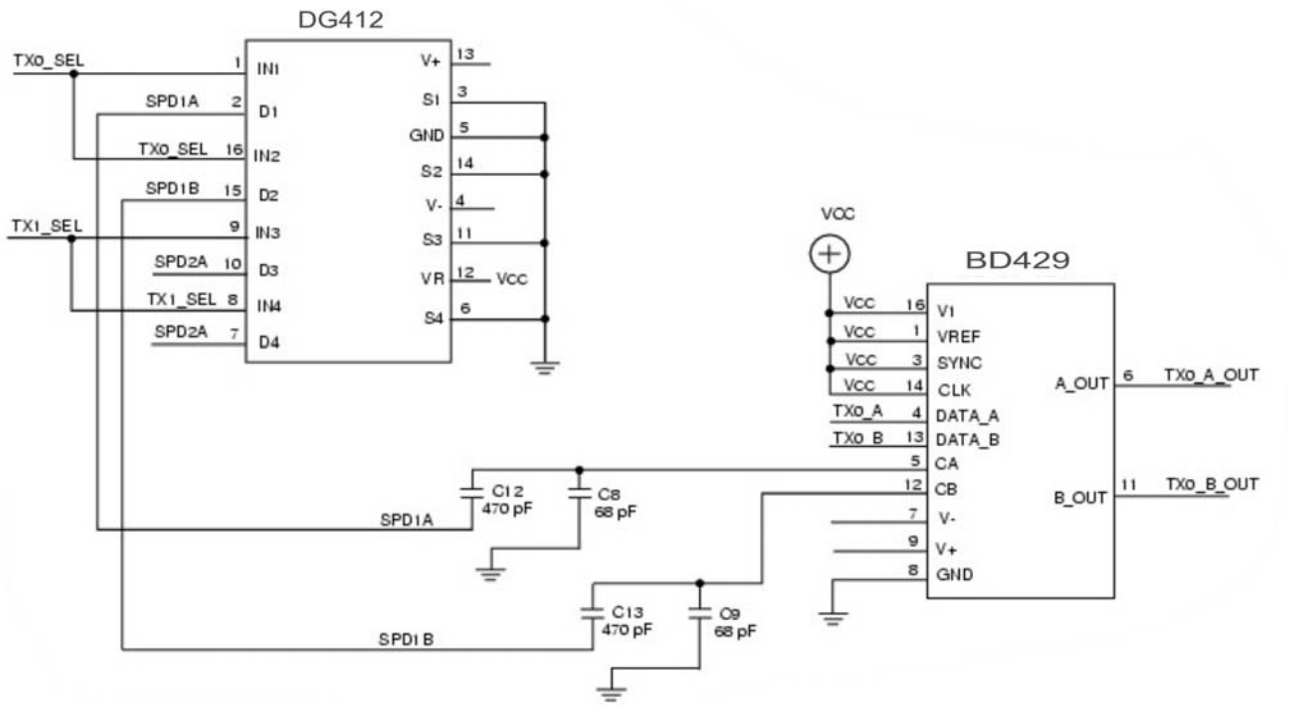


Figure 8: Typical Circuitry- Switching Capacitors For High-Speed/Low-Speed Operation

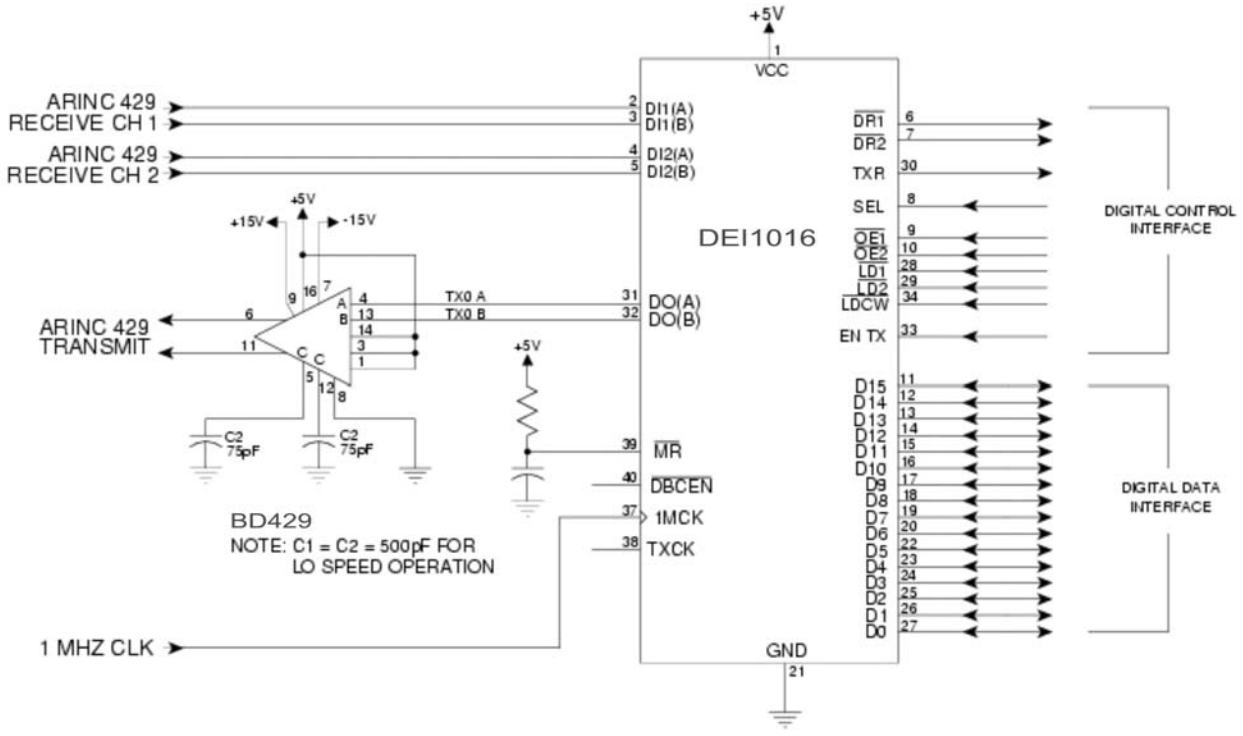
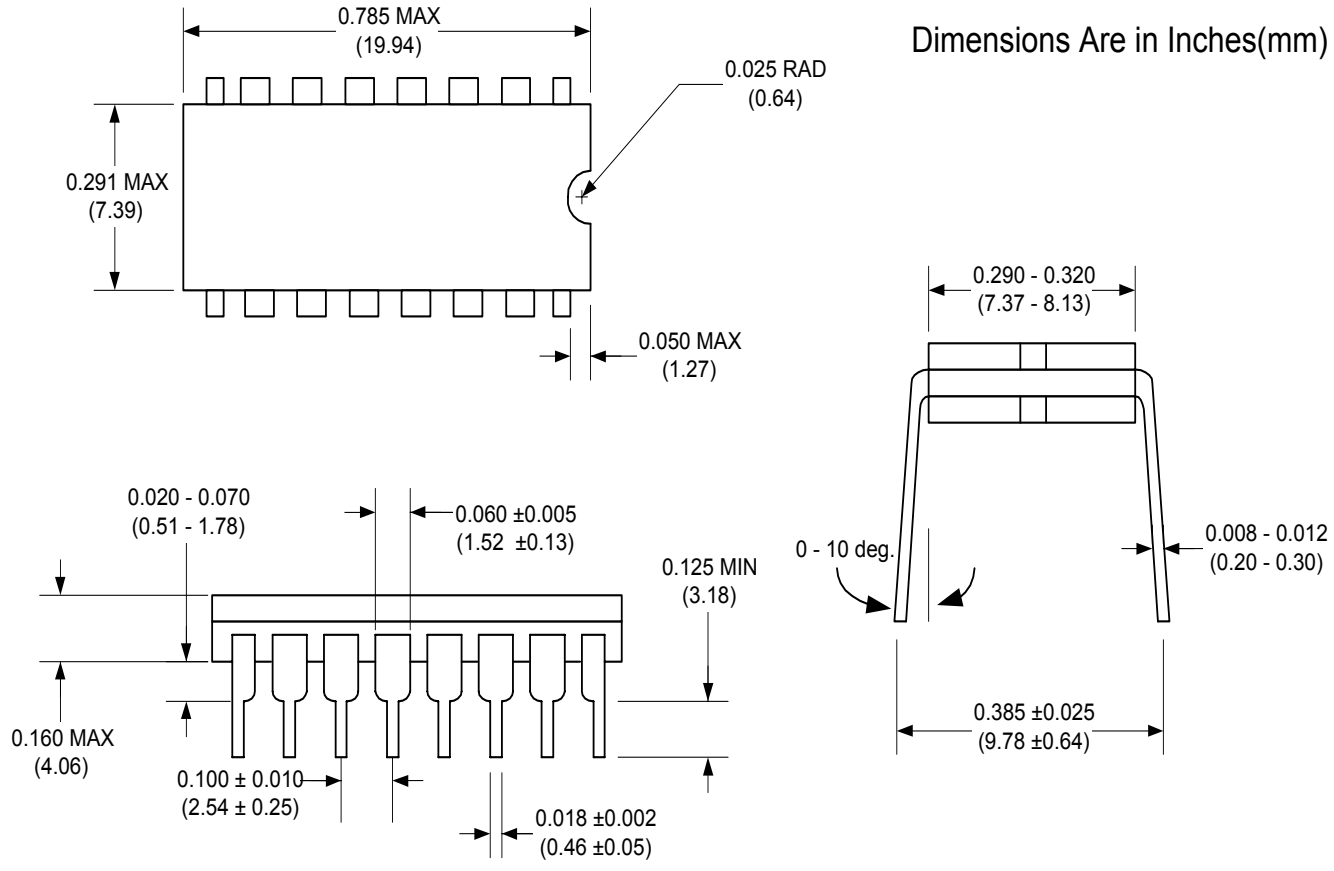
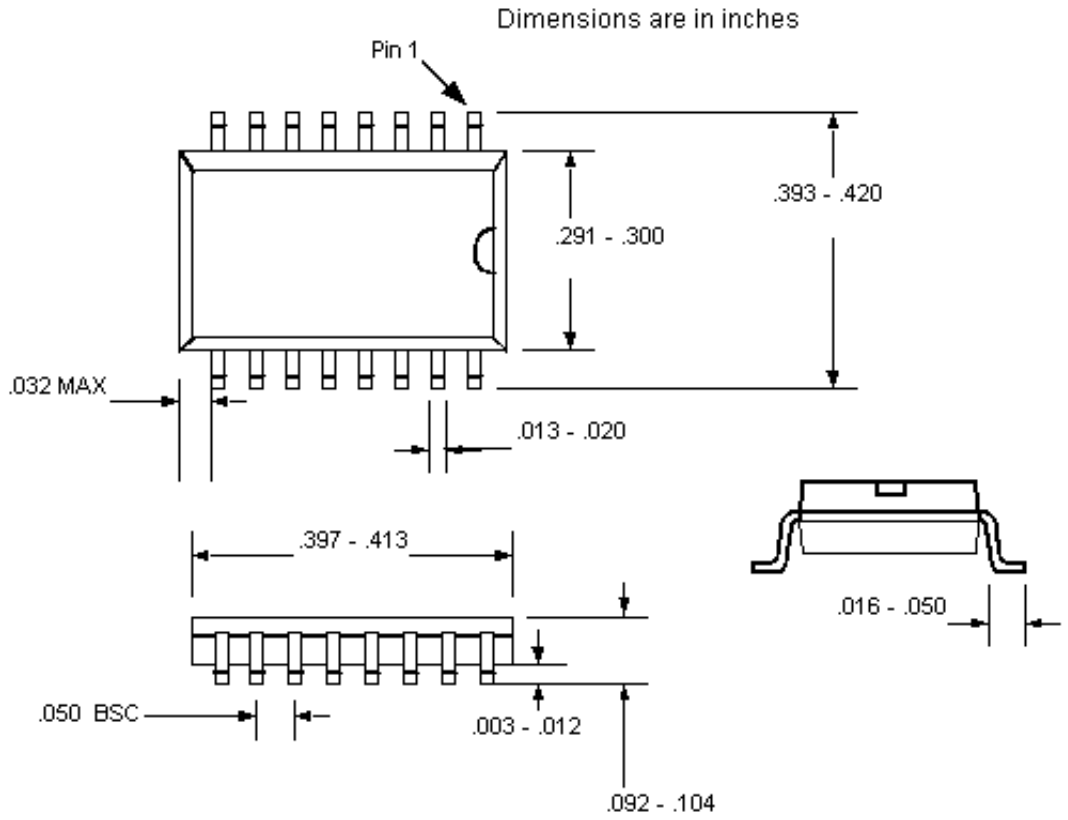


Figure 9: Typical Transceiver/Line Driver Interconnect Configuration

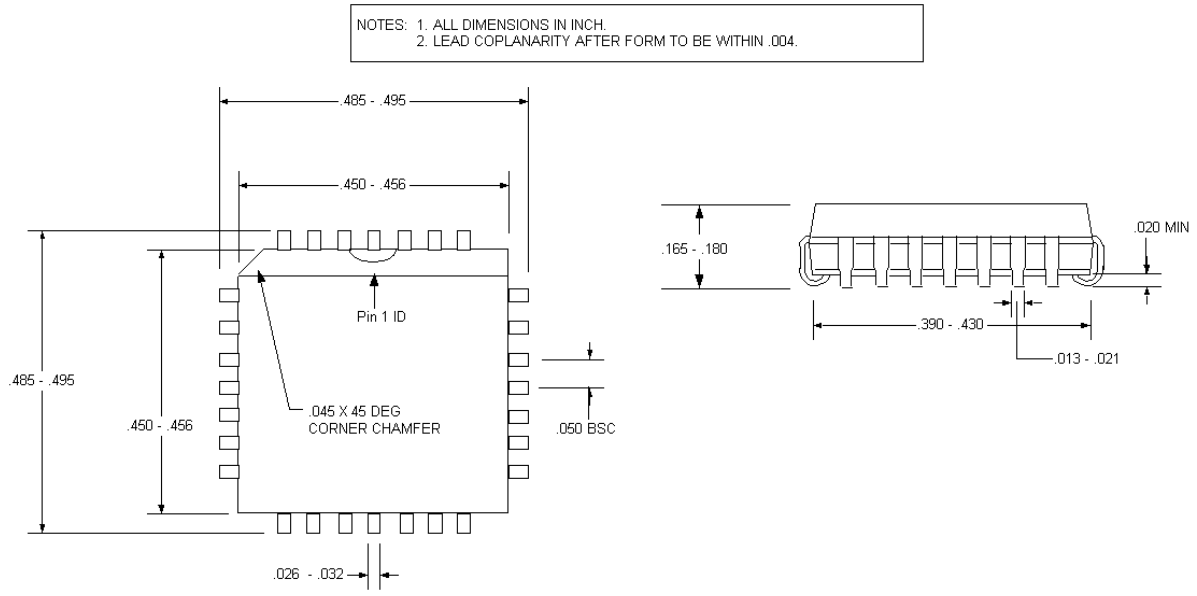
Table 10: BD429 Package Characteristics Table					
PACKAGE TYPE	16 Lead Ceramic Dip	16 Lead Plastic Dip	16 Lead SOIC Wide Body	16 Lead Ceramic SOP	28 Lead PLCC
REFERENCE	16 CERDIP	16 PDIP	16 SOIC WB	16 CSOP	28 PLCC
THERMAL RESISTANCE:					
θ_{JA} °C/W	75	70	75 (4 layer PCB)	TBD	55 (4 layer PCB)
θ_{JC} °C/W	35	34	25	23	25
JEDEC MOISTURE SENSITIVITY LEVEL	N/A Hermetic	N/A Thru-Hole	2	N/A Hermetic	3
JEDEC REFERENCE	MS-030-AC	MS-001-BB	MS-013-AA	N/A	MS-018-AB



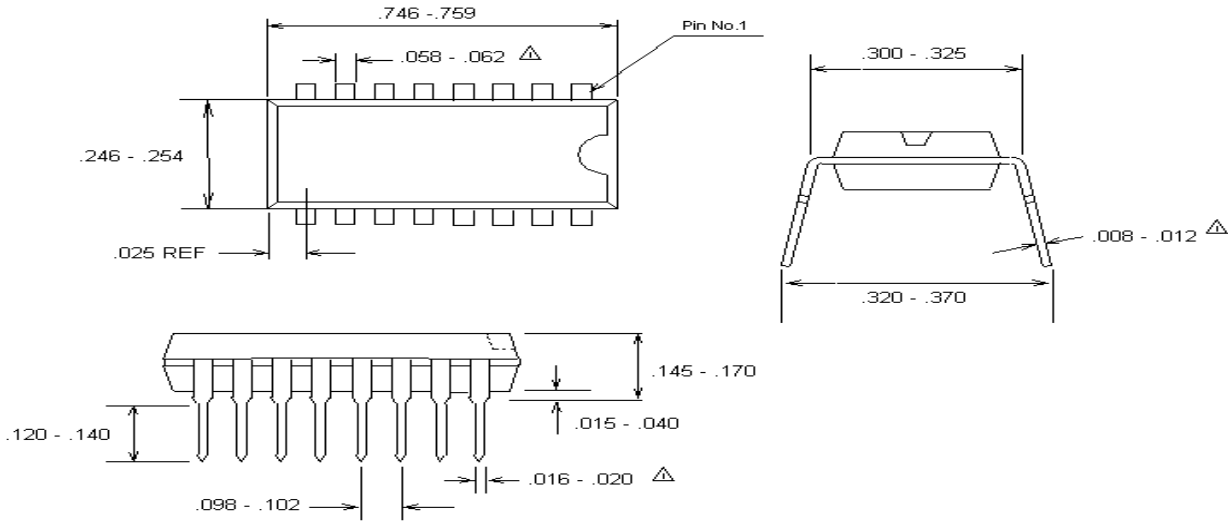
16 Pin CERDIP Package Dimensions



16 Lead SOIC WB Package Dimensions



28 Lead PLCC Package Dimensions



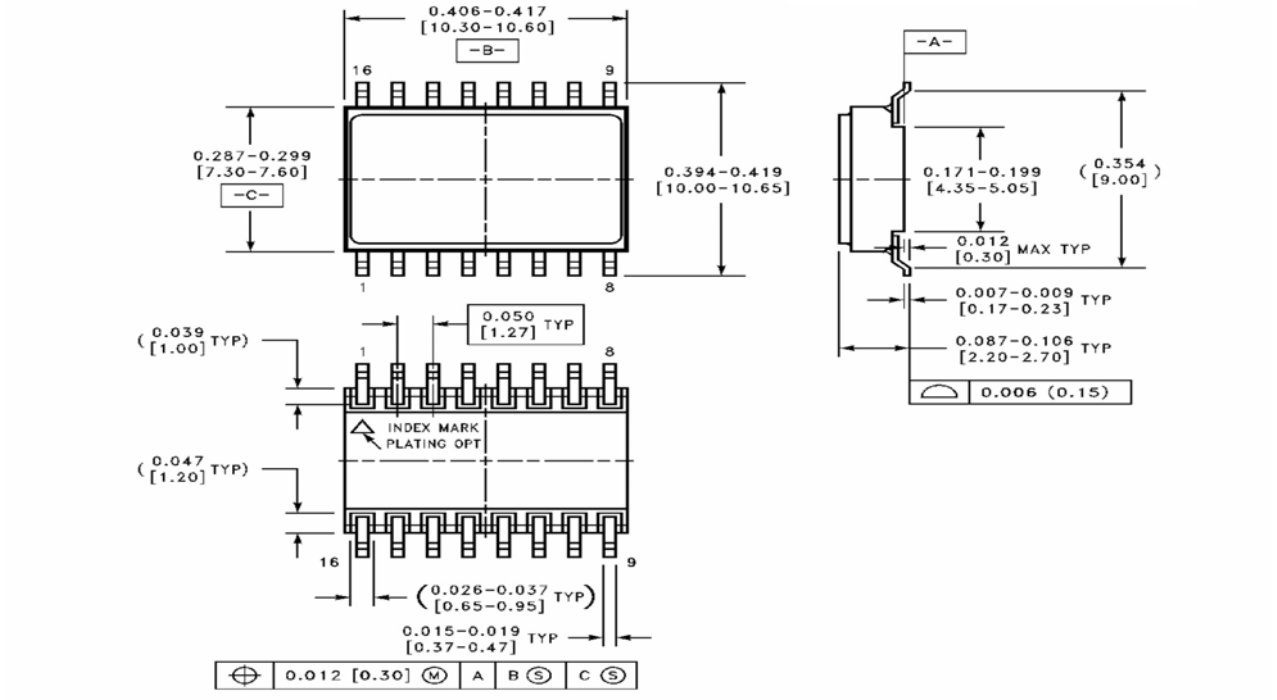
Notes:

⚠ Spade Width, Lead Width,and Lead Thickness exclusive of tin plating or solder dipping thickness.

Dimensions are in Inches

16 Pin PDIP Package Outline

Dimensions are in Inches



16 Lead CSOP Package Outline

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